CCSDS / ECSS
Telemetry Encoder and Telecommand Decoder

AEROFLEX GAISLER

Description

The Telemetry Encoder and Telecommand Decoder concept developed by Aeroflex Gaisler implements part of the protocol layers in hardware (IP cores) and part in software (operating system drivers and protocol stacks). The concept is complemented by specially developed hardware suitable for telemetry and telecommand on-board and ground segment developments.

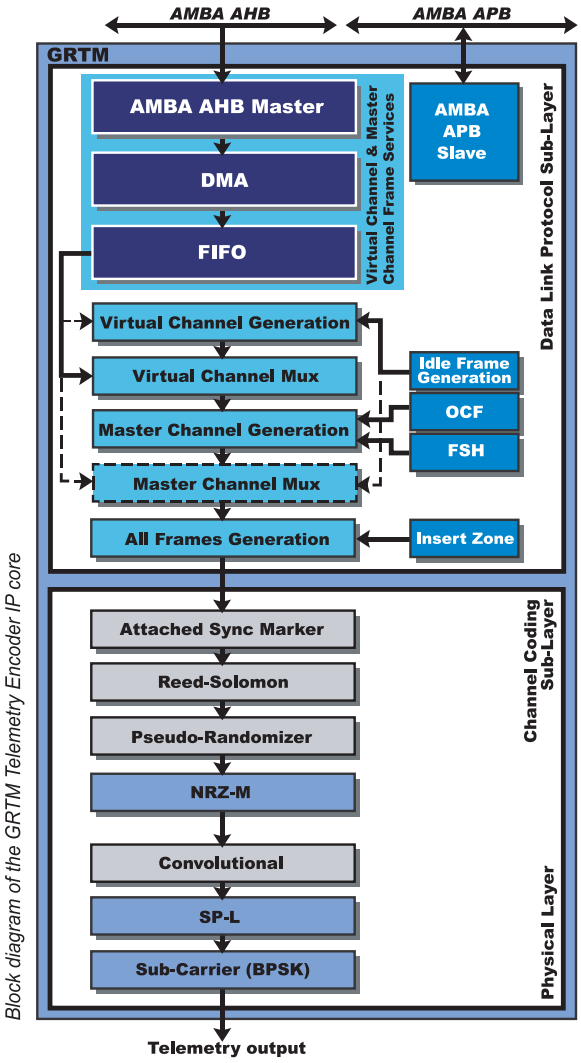
Hardware features

The Telemetry Encoder IP core implements:

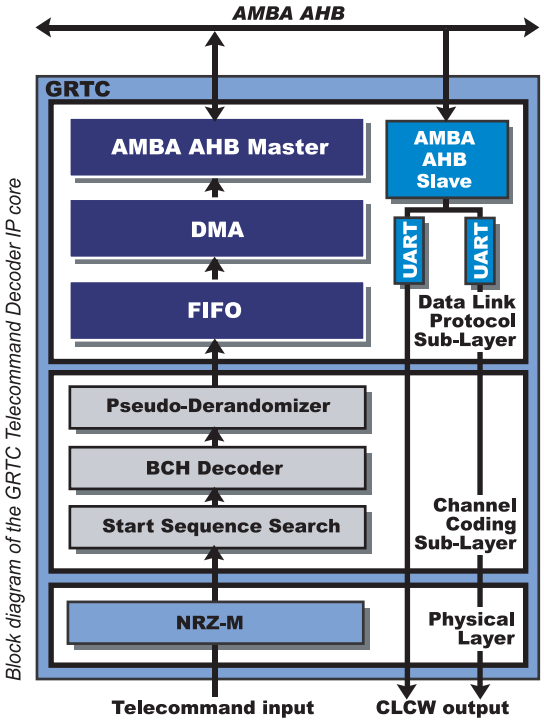
- Packet Telemetry (TM) and Advanced Orbiting Systems (AOS)
- Data Link - Protocol Sub-Layer:
  - Virtual / Master Channel Frame Service (DMA support)
  - Virtual Channel Generation
  - Virtual Channel Multiplexing
  - Master Channel Generation
  - Master Channel Multiplexing (with Idle Frames)
  - All Frames Generation (FHEC, FECF, etc.)
- Data Link - Synchronization and Channel Coding Sub-Layer:
  - Attached Synchronization Marker
  - Reed-Solomon encoding (E=8 and E=16)
  - Pseudo-Randomizer
  - Convolutional coding with/without puncturing
- Physical Layer:
  - Non-Return-to-Zero Mark modulation (NRZ-M)
  - Split-Phase Level modulation (SP-L)
  - Sub-Carrier modulation (BPSK)
- Compatibility:
  - CCSDS 131.0-B-1, 132.0-B-1, 133.0-B-1 and 732.0-B-2
  - ECSS-E-50-01A, ECSS-E-50-03A and ECSS-E-50-05A
  - ESA PSS-04-103, PSS-04-105 and PSS-04-106

The Telecommand Decoder IP core implements:

- Packet Telecommand (TC)
- Data Link - Protocol Sub-Layer:
  - Provides DMA support from lower sub-layer
- Data Link - Synchronization and Channel Coding Sub-Layer:
  - Pseudo-Derandomization
  - BCH codeblock decoding
  - Start Sequence Search
- Physical Layer:
  - Non-Return-to-Zero Mark de-modulation (NRZ-M)
- Compatibility
  - CCSDS 231.0-B-1, 232.0-B-1 and 232.1-B-1
  - ECSS-E-50-04A and ECSS-E-50-05A
  - ESA PSS-04-105, PSS-04-107 and PSS-04-151



Block diagram of the GRTM Telemetry Encoder IP core



Block diagram of the GRTC Telecommand Decoder IP core

Software features

The software part of the Telemetry Encoder and the Telecommand Decoder comprises drivers for the real-time operating systems RTEMS and Windriver VxWorks. The drivers provide basic configuration and communication with the IP cores, facilitating DMA handling etc. The higher protocol layers of the two standards are implemented in the application domain as independent protocol stacks.

The Telemetry Encoder software implements:

- Data Link - Protocol Sub-Layer:
  - Packet Processing (only Idle Packet generation)
  - Virtual Channel Generation
  - Virtual Channel Multiplexing (bandwidth allocation)
  - Virtual and Master Channel Frame Services
  - Support for Frame Secondary Header (FSH) and Operational Control Field (OCF)

The Telecommand Decoder software implements:

- Data Link - Protocol Sub-Layer:
  - Virtual Channel Reception:
    - Communications Operation Procedure-1 (COP-1)
    - Frame Acceptance and Reporting Mechanism (FARM)
    - Support for Command Link Control Word (CLCW)
  - Virtual Channel Demultiplexing
  - Master Channel Demultiplexing
  - All Frames Reception

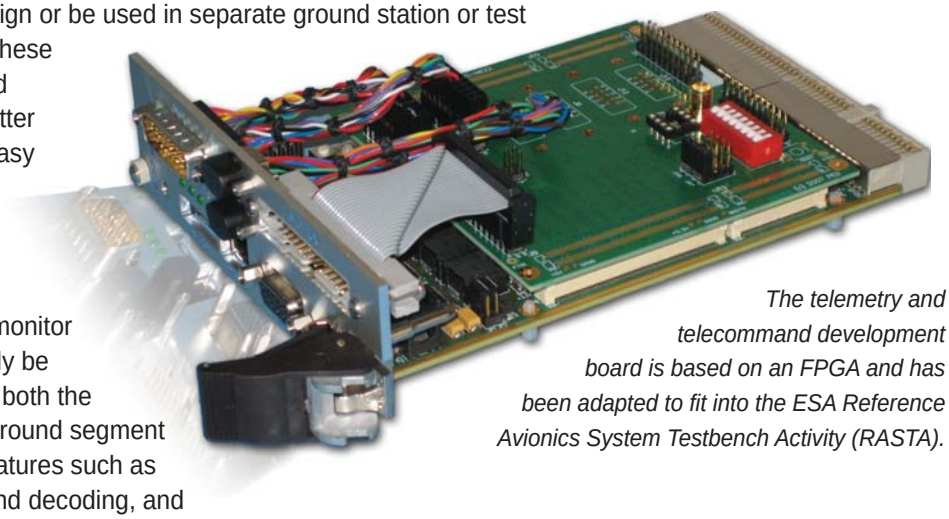
Development board

An FPGA development board has been designed especially to support the development and fast prototyping of telemetry and telecommand systems. The board incorporates a large capacity Xilinx Virtex-4™ or Actel RTAX2000S/AX2000 field programmable gate array and is capable of operating either as a stand-alone board, or as a compact PCI plug-in card in either the System slot or Peripheral slots. Expansion to user's peripherals and circuits can be implemented in an adjacent slot via the PCI interface. The board features connectors (RS422 levels) directly compatible with popular test equipment and interfaces such as SpaceWire (LVDS).

Whilst the board is perfectly suitable as a general-purpose development platform for any FPGA project, the incorporation of on-board volatile (SRAM and SDRAM) and non-volatile memories (FLASH) makes the board ideal for implementing Telemetry, Telecommand and LEON3 or LEON4 based designs.

Tools

The IP cores and software have been developed to match the Fault Tolerant LEON3 and LEON4 32-bit SPARC processors and the Aeroflex Gaisler GRLIB IP library that provides a rich variety of IP cores for demanding space applications. To complement the IP cores targeted towards the space segment, additional IP cores for the ground segment are available that can be integrated in any GRLIB based system-on-a-chip design or be used in separate ground station or test equipment designs. These telemetry receiver and telecommand transmitter IP cores provide an easy way to interface the corresponding space segment IP cores.



The telemetry and telecommand development board is based on an FPGA and has been adapted to fit into the ESA Reference Avionics System Testbench Activity (RASTA).

The GRMON debug monitor software can optionally be configured to support both the space segment and ground segment IP cores, providing features such as telemetry reception and decoding, and telecommand encoding and transmission, effectively providing similar services as a simple ground station.

The Consultative Committee CCSDS.ORG for Space Data Systems

ECSS

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