

# Master Thesis Proposal – Porting NetBSD to the LEON/GRLIB System-on-Chip SPARCv8 architecture

## Background

Aeroflex Gaisler develops and supports the GRLIB integrated VHDL IP library. The library is freely available in open-source, and includes blocks such as the LEON3 SPARC V8 processor, PCI, USB host/device controllers, CAN, DDR and Ethernet interfaces. The AMBA on-chip bus is used as the standard communication interface between the GRLIB cores.

Part of GRLIB is the fault-tolerant LEON3/4 32-bit SPARCv8 compatible processor designed for aerospace and commercial embedded systems. Real-time operating systems that is supported by the LEON is for example RTEMS, VxWorks, ThreadX, Nucleus and eCos. Aeroflex Gaisler has supported Linux 2.0, 2.6 and recently announced the support for the 3.x kernel series.

The NetBSD UNIX-like operating system is a very mature operating system that has been designed with portability in mind. Its huge software library and BSD-license is appealing. The NetBSD project claims to have created the most portable OS in the world, it already have Tier II support for the SPARCv8 architecture but not for the LEON implementation of SPARC.

## Project description

The work will consist of porting NetBSD to a single-core LEON System-on-Chip platform. The LEON is a specific implementation of the SPARCv8 specification that must be described within the NetBSD operating system to fully function. Basic peripherals such as IRQ Controller and Timer requires a basic driver in NetBSD. The current NetBSD SPARC architectural port makes low-level operations by calling on a SUN boot loader which has already been developed in-house for the LEON within the Linux 2.6/3.x projects, MKLINUXIMG. The MKLINUXIMG boot loader may require minor modifications in order to boot the NetBSD kernel.

The student(s) have to access to an advanced hardware debugger (GRMON2), simulators (TSIM2) and a deep in-house experience and knowhow of porting other operating systems listed in the background section. The open-source implementations of Linux and RTEMS can serve as an aid during the work.

The main goal of the project is to boot NetBSD as far as possible on a single-core LEON system.

## Qualification

The applicant(s) should have strong interest in low-level or operating system software design, and be familiar with the C programming language and any assembly language. The work is suitable for one, possibly two students. Support and mentoring will be provided by the supervisor and other Aeroflex Gaisler staff.

## Contact

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The logo for Aeroflex Gaisler features a large, stylized letter 'A' on the left. The top of the 'A' is a thick black arch, and the bottom is a teal inverted triangle. To the right of the 'A', the word 'AEROFLEX' is written in a bold, black, sans-serif font. Below 'AEROFLEX', the word 'GAISLER' is written in a teal, sans-serif font.

# AEROFLEX

## GAISLER

Aeroflex Gaisler AB is a provider of system-on-chip (SoC) solutions for exceptionally competitive markets such as aerospace, military and demanding commercial applications. Aeroflex Gaisler's products consist of user-customizable 32-bit SPARC V8 processor cores, peripheral IP-cores and associated software and development tools. Aeroflex Gaisler solutions help companies develop highly competitive customer and application-specific SoC designs, as well as providing radiation-hardened components for the space market.

The key product is the LEON synthesizable processor model together with a full development environment and a library of IP cores (GRLIB). The LEON processor and the library of IP cores are highly configurable, and are suitable for system-on-chip designs. The processor combines high performance and an advanced architecture with low gate count and low power consumption. Implementing the SPARC V8 architecture (IEEE-1754), the LEON processor offers a truly open and well supported instruction set. The processor and the IP-core library can favorably be used in a large range of applications.

Aeroflex Gaisler's LEON-FT processor implements unique fault-tolerance features that allow it to function correctly in the severe space environment. The processor includes on-chip error-detection and error-correction logic to detect and remove any soft error caused by cosmic radiation.

Our personnel have extended design experience, and have been involved in establishing European standards for ASIC and FPGA development. We have a long experience in the management of ASIC development projects, and in the design of flight quality microelectronic devices. The company specializes in digital hardware design (ASIC/FPGA) for both commercial and aerospace applications.

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