Master Thesis Proposal – Implementing hardware supported break/watch -pointing for LEON SPARC Linux 3.x

Background

Aeroflex Gaisler develops and supports the GRLIB integrated VHDL IP library. The library is freely available in open-source, and includes blocks such as the LEON3 SPARC V8 processor, PCI, USB host/device controllers, CAN, DDR and Ethernet interfaces. The AMBA on-chip bus is used as the standard communication interface between the GRLIB cores.

Part of GRLIB is the fault-tolerant LEON3/4 32-bit SPARCv8 compatible processor designed for aerospace and commercial embedded systems. LEON software is typically debugged with the in-house developed hardware debugger GRMON, that controls the CPU execution via a Debug Support Unit (DSU). Operating systems often provide means for natively debugging user space applications without requiring additional hardware by providing a debugging API to applications. The open-source GNU GDB debugger is an example of an application debugger accessing such an API. In order for the operating system to implement the API it requires support from the architectural layer. Currently the Linux SPARC architecture does not support hardware assisted break/watch-pointing, but supports other debugging functionality required for GDB to operate.

Project description

The work will consist of adding support for LEON hardware assisted breakpoint and watchpoint functionality to the SPARC architecture of Linux 3.x and testing it using GDB running on the LEON CPU. This requires that the Linux SPARC 32-bit architecture is extended with the necessary support and that the LEON specific hardware is described, initialized and required trap handlers implemented.

The student(s) have access to an advanced hardware debugger (GRMON2) for debugging the Linux kernel and a deep in-house experience and knowhow about the LEON hardware and Linux kernel.

The main goal of the project is to implement Linux support for hardware assisted break/watch -pointing on the LEON and if time allows submit it to the mainline Linux kernel at www.kernel.org.

There are other LEON Linux kernel projects too that can be subject for a master thesis, such as improving the SPARC virtual I/O address allocation management by using the generic Linux kernel management instead of relying on a custom SPARC implementation.

Qualification

The applicant(s) should have strong interest in low-level or operating system software design, and be familiar with the C programming language. The work is suitable for one students. Support and mentoring will be provided by the supervisor and other Aeroflex Gaisler staff.

Contact

Daniel Hellstrom (supervisor)
Aeroflex Gaisler, Kungsgatan 12, 411 19 Göteborg, Tel +46 31 7758657
www.gaisler.com

AEROFLEX GAISLER

Aeroflex Gaisler AB is a provider of system-on-chip (SoC) solutions for exceptionally competitive markets such as aerospace, military and demanding commercial applications. Aeroflex Gaisler's products consist of user-customizable 32-bit SPARC V8 processor cores, peripheral IP-cores and associated software and development tools. Aeroflex Gaisler solutions help companies develop highly competitive customer and application-specific SoC designs, as well as providing radiation-hardened components for the space market.

The key product is the LEON synthesizable processor model together with a full development environment and a library of IP cores (GRLIB). The LEON processor and the library of IP cores are highly configurable, and are suitable for system-on-chip designs. The processor combines high performance and an advanced architecture with low gate count and low power consumption. Implementing the SPARC V8 architecture (IEEE-1754), the LEON processor offers a truly open and well supported instruction set. The processor and the IP-core library can favorably be used in a large range of applications.

Aeroflex Gaisler's LEON-FT processor implements unique fault-tolerance features that allow it to function correctly in the severe space environment. The processor includes on-chip error-detection and error-correction logic to detect and remove any soft error caused by cosmic radiation.

Our personnel have extended design experience, and have been involved in establishing European standards for ASIC and FPGA development. We have a long experience in the management of ASIC development projects, and in the design of flight quality microelectronic devices. The company specializes in digital hardware design (ASIC/FPGA) for both commercial and aerospace applications.

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