

LEON-XCKU-EX

SPARC V8 Processor

2020 User's Manual

The most important thing we build is trust

COBHAM

Features

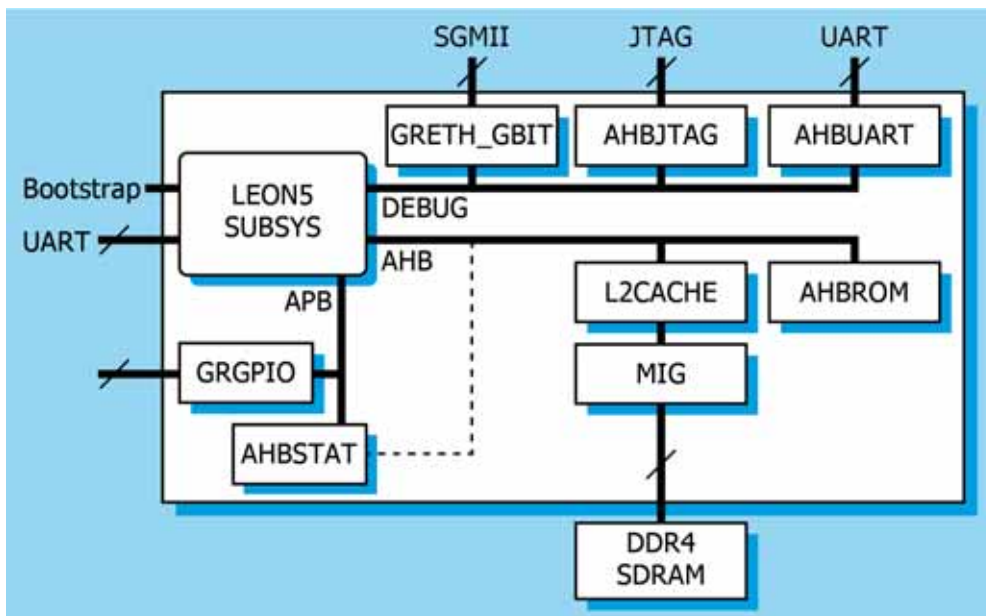
- SPARC V8e integer unit(s) with dual-issue pipeline, 16 KiB instruction and 16 KiB data caches, hardware multiplier and divider, power-down mode, hardware watchpoints, etc.
- Double precision IEEE-754 floating point unit
- Memory management unit
- Advanced on-chip debug support unit
- Level-2 cache
- DDR4 SDRAM
- UART, Timers, GPIO port, Interrupt controller, Status registers
- Ethernet 10/100/1000 Mbit MAC interface

Description

The LEON-XCKU FPGA bitstreams are a collection of example designs built from Cobham Gaisler's GRLIB IP library using a template design for Xilinx Kintex Ultrascale devices. The example designs are suitable for evaluation of LEON microprocessors in system-on-chip designs.

Specification

- Targets Xilinx Kintex Ultrascale KC105 Evaluation Kit FPGA board
- 100 MHz system frequency



Applications

The LEON/GRLIB template designs can be adapted as multiple configurations, covering instrument, payload and control applications.

SPARC

Table of contents

1	Introduction.....	3
1.1	Scope.....	3
1.2	Document revision history.....	3
1.3	Reference documents.....	3
2	Example designs.....	4
2.1	Overview.....	4
2.2	Configurations.....	5
3	Architecture.....	6
3.1	Cores.....	6
3.2	Interrupts.....	6
3.3	IP core documentation.....	7
3.4	Signals.....	8
3.5	Resource utilization.....	8
4	Working with the board.....	9
4.1	Prerequisites.....	9
4.2	Programming the FPGA device and connecting with GRMON3.....	9
4.3	Support.....	9
5	Ordering information.....	10

1 Introduction

1.1 Scope

The LEON line of processors and the GRLIB IP library has support for Xilinx Kintex Ultrascale devices. This support consists of a techmap layer that wraps specific technology elements such as memory macros and pads. GRLIB also contains a template designs for developments boards such as the Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit and infrastructure that automatically builds project files for Xilinx Vivado and synthesis tools such as Mentor Precision Hi-Rel and Synopsys Synplify Premier.

This document describes a set of ready-made FPGA configurations (bitstreams) that have been built from the GRLIB template designs.

1.2 Document revision history

Table 1. Change record

Version	Date	Note
1.0	2019 December	First issue

1.3 Reference documents

- [AMBA] AMBA™ Specification, Rev 2.0, ARM IHI 0011A, 13 May 1999, Issue A, first release, ARM Limited
- [GRLIB] GRLIB IP Library User's Manual, Cobham Gaisler, www.Cobham.com/gaisler
- [GRIP] GRLIB IP Core User's Manual, Cobham Gaisler, www.Cobham.com/gaisler
- [QSG] LEON-XCKU-EX Quick Start Guide, LEON-XCKU-EX-QSG, www.gaisler.com/LEON-XCKU

2 Example designs

2.1 Overview

The LEON-XCKU-EX example designs are based on a common architecture. The architecture is centered around the AMBA [AMBA] Advanced High-speed Bus (AHB), to which the processor(s) and other high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge. The architecture for the basic design is shown in figure 1.

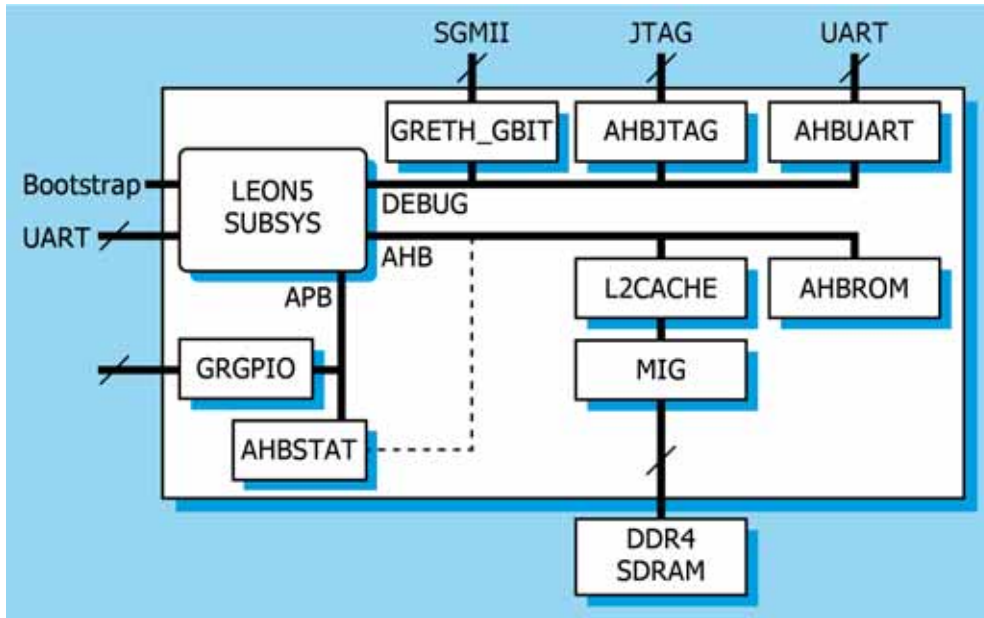


Figure 1. Architectural block diagram of LEON-XCKU-EX1

The full LEON-XCKU-EX architecture includes the following modules:

- LEON5 SPARC V8e Integer Unit with 16 KiB instruction cache and 16 KiB data cache. IEEE-754 Floating Point Unit and Memory Management Unit.
- Debug Support Unit with UART, Ethernet, and JTAG Debug Links
- Level-2 cache controller
- Xilinx MIG DDR4 SDRAM controller
- Timer unit with two 32-bit timers
- Interrupt controller for 15 interrupts in two priority levels
- UART with FIFO and separate baud rate generator
- General purpose I/O port (GPIO).
- AMBA AHB status register (not included in all EX variants)

The GRLIB IP library contains a template design that has been used as the base for LEON-XCKU-EX designs. The template design can easily be extended to add additional GRLIB IP library IP cores such as:

- Memory controllers with EDAC
- SpaceWire links with CRC support and hardware RMAP target
- SpaceFibre links
- CAN-2.0 controllers
- Mil-Std-1553 BC/BM/RT

A full list of GRLIB IP library components can be found in [GRIP]. The GRLIB user's manual is available on-line [GRLIB].

2.2 Configurations

The bitstream is available for download from <https://www.gaisler.com/LEON-XCKU>

Table 2. Example configurations

Configuration name	EX1	EX2	EX3	EX4
XCKU device	040 (KC105)	040 (KC105)	040 (KC105)	040 (KC105)
Processor	LEON5	LEON5	LEON5	LEON5
Number of processor cores	1	1	2	4
Level-1 cache	16+16 KiB	16+16 KiB	16+16 KiB	16+16 KiB
Hardware multiply÷	Yes	Yes	Yes	Yes
Multiply & accumulate	No	No	No	No
Single-vector trapping	Yes	Yes	Yes	Yes
Power down mode	Yes	Yes	Yes	Yes
Memory Management Unit	Yes	Yes	Yes	Yes
Floating Point Unit	GRFPU5	NanoFPU	GRFPU	NanoFPU
Debug Support Unit	Yes	Yes	Yes	Yes
Level-2 cache	Yes	Yes	Yes	Yes
UART Debug Link	Yes	Yes	Yes	Yes
JTAG Debug Link	Yes	Yes	Yes	Yes
Ethernet MAC 10/100/1000 Mbit	Yes	Yes	Yes	Yes
Memory Controller	Xilinx DDR4 MIG	Xilinx DDR4 MIG	Xilinx DDR4 MIG	Xilinx DDR4 MIG
Standard peripherals	Yes	Yes	Yes	Yes

Note: The configurations above are examples on how to use the GRLIB IP cores on Xilinx Kintex Ultrascale. All IP cores have several configuration parameters and are individually configurable.

Note: While software may report that fault-tolerance is enabled for the example designs, the bitstreams are not suitable for use in environments with radiation effects.

3 Architecture

3.1 Cores

The common architecture is based on cores from the GRLIB IP library. The vendor and device identifiers for each core can be extracted from the plug & play information. The used IP cores are listed in table 3.

Table 3. Used IP cores

Core	Function	Vendor	Device
AHBCTRL	AHB Arbiter & Decoder	0x01	-
APB3CTRL	AHB/APB3 Bridge	0x01	0x0A2
APBCTRL	AHB/APB Bridge	0x01	0x006
LEON3FT	LEON3 SPARC V8 32-bit processor	0x01	0x053
DSU3	LEON3 Debug support unit	0x01	0x004
L3STAT	LEON3 Performance counters	0x01	0x098
LEON4	LEON4 SPARC V8 32-bit processor	0x01	0x048
DSU4	LEON4 Debug support unit	0x01	0x049
L4STAT	LEON4 Performance counters	0x01	0x047
LEON5	LEON5 SPARC V8 32-bit processor	0x01	0x0BA
DSU5	LEON5 Debug support unit	0x01	0x0BB
L5STAT	LEON5 Performance counters	0x01	0x0B9
AHBUART	Serial/AHB debug interface	0x01	0x007
AHBJTAG	JTAG/AHB debug interface	0x01	0x01C
AHBSTAT	AHB failing address register	0x01	0x052
APBUART	8-bit UART with FIFO	0x01	0x00C
GPTIMER	Modular timer unit with watchdog	0x01	0x011
IRQMP	LEON3 Interrupt controller	0x01	0x00D
GRGPIO	General purpose I/O port	0x01	0x01A
L2CACHE	Level-2 Cache Controller	0x01	0x04B
Xilinx MIG	Xilinx DDR4 MIG - with GRLIB wrapper	0x01	0x090

Note that the table above lists IP cores used in the full set of planned LEON-XCKU-EX designs. Several designs contain a subset of the IP cores in the table.

3.2 Interrupts

The LEON-XCKU-EX example designs use the same interrupt assignment for all configurations. See the description of the individual cores for how and when the interrupts are raised. All interrupts are handled by the interrupt controller and forwarded to the processor.

Table 4. Interrupt assignment

Core	Interrupt	Comment
AHBSTAT	4	Not included in all EX variants
APBUART	2	
GPTIMER	8, 9	
GRETH_GBIT	5	

3.3 IP core documentation

This user manual does not contain IP core documentation. Please refer to the GRLIB IP Core User's Manual [GRIP] available at <http://gaisler.com/products/grlib/grip.pdf>.

The GRMON debug monitor also provides information about the system-on-chip's configuration via the command **info sys**.

3.4 Signals

Please see the LEON-XCKU-EX Quick Start Guide [QSG] for information on FPGA pinout.

3.5 Resource utilization

Resource utilization is described in the GRLIB area spreadsheet, available at:

https://www.gaisler.com/products/grlib/grlib_area.xls

4 Working with the board

4.1 Prerequisites

The following items are required to use LEON-XCKU-EX designs:

- Workstation with Windows or Linux
- Xilinx KCU105 Evaluation Kit
- LEON-XCKU bitstream
- GRMON3 debug monitor

The two last items can be downloaded via <http://gaisler.com/LEON-XCKU>.

Cobham Gaislers standard offer of toolchains can be used to build and run software on the LEON-XCKU-EX designs. Toolchains and run-time environments are available for download via <http://gaisler.com>.

4.2 Programming the FPGA device and connecting with GRMON3

Please see the LEON-XCKU-EX Quick Start Guide [QSG] for information on FPGA programming and using the SoC design.

4.3 Support

In case of technical issues please contact support@gaisler.com. The support line is normally available only to companies and institutions with active support contracts. Limited support for the LEON-XCKU-EX example designs is provided. When contacting support please provide a clear description of which design that is used and your affiliation.

Sales and licensing questions should be directed to sales@gaisler.com.

5 Ordering information

Please contact sales@gaisler.com for information on the GRLIB IP library.

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