

LEON3-FT

RT ProASIC3



Introduction

The LEON3-FT processor is available as a standard component using the Actel RT ProASIC3 Field Programmable Gate Array. The fault tolerant design of the processor in combination with the radiation tolerant FPGA makes it ideally suited for space and other high-rel applications.

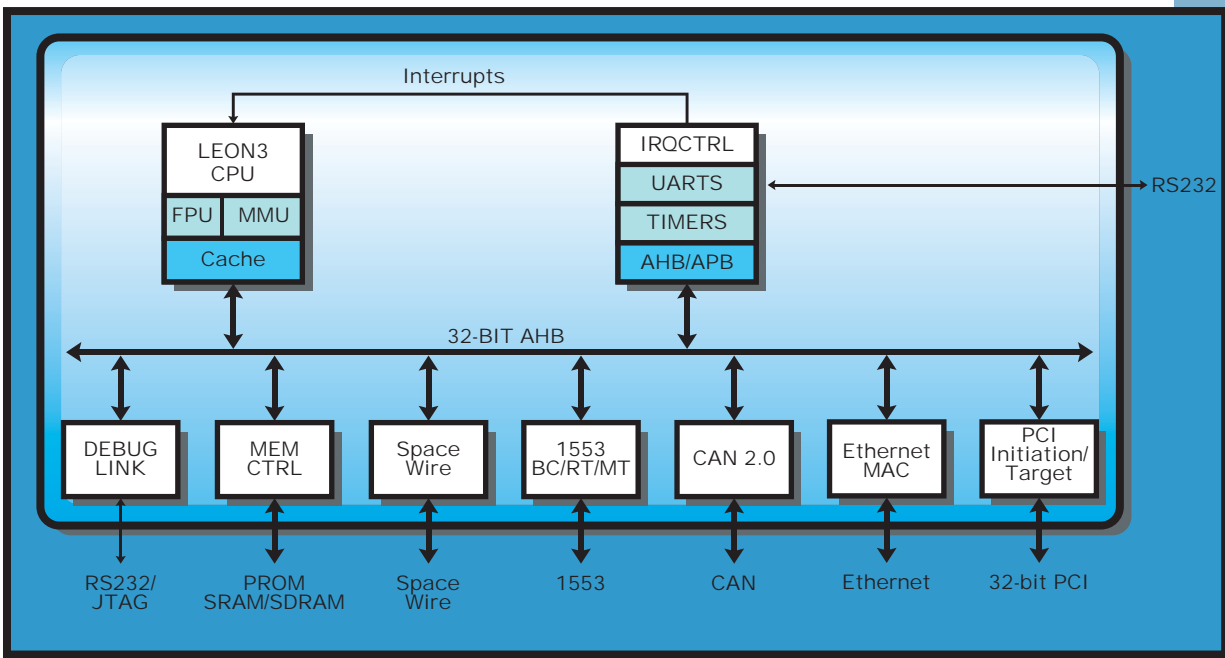
The LEON3-FT is a 32-bit processor based on the SPARC V8 architecture. The floating point unit provides support for both single- and double-precision floating point operations. A unique debug interface allows non-intrusive hardware debugging and provides access to all on-chip registers and memory.

The processor is currently used in European and international space programmes and has been successfully validated and qualified. A complete software development environment including compilers, debuggers and operating systems is freely available for download at www.aeroflex.com/gaisler.

Prototyping is possible using the commercial version ProASIC3L FPGA on a development board.

Main Features

- SPARC V8 integer unit with 7-stage pipeline
- Hardware multiply and divide
- Separate instruction and data caches
- Memory management unit
- Double precision IEEE-754 compliant floating point unit
- EDAC protected interface to 8/16/32-bit PROM/SRAM/SDRAM
- Advanced on-chip debug support unit
- UART, timer unit, GPIO port
- Mil-Std-1553B, SpaceWire and CAN 2.0B bus
- Ethernet MAC
- PCI Initiater/Target/Arbiter
- Power down mode



Availability

The LEON3-FT on the Actel RT ProASIC3 RT3PE3000L device is available in several different standard configurations tailored for spacecraft and instrument control. Other configurations can be offered on request. The components can be pre-programmed and are shipped with a complete data sheet and user's manual. For evaluation and prototyping the commercial version ProASIC3L A3PE3000L FPGA is available. The high-rel version is available in B flow. For price and ordering please contact Aeroflex Gaisler.

Standard configurations

Configuration name	Instrument Controller -1	Instrument Controller -2	Spacecraft Controller -1	Spacecraft Controller -2	Spacecraft Controller -3	Spacecraft Controller -4	Payload Controller -1	Payload Controller -2
Configuration ID (CID)	1	2	3	4	5	6	7	8
LEON3FT Integer Unit	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hardware multiply & divide					Yes	Yes		Yes
Power down mode	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Memory Management Unit					Yes	Yes		
Floating Point Unit	Yes	Yes	Yes				Yes	Yes
Debug Support Unit	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
UART Debug Link								
JTAG Debug Link	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
On-Chip Memory	4 kBytes		4 kBytes					
1553 RT	1							
1553 BC/RT/MT			1					
SpaceWire		2		3	2		2	
CAN 2.0B	1				1			
PCI Initiator/Target/Arbiter						Yes		
Ethernet MAC						1		2
Memory Controller	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SDRAM Controller				Yes	Yes	Yes	Yes	Yes
Reed-Solomon for SDRAM option				Yes	Yes	Yes	Yes	
Standard Peripherals	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package	CCGA484 / LGA484							

Specifications	
Clock speed	20 / 25 MHz / 33 MHz PCI
Integer Performance	20 DMIPS
Floating Point Performance	4 MFLOPS
Power consumption	200 mW (TBD)
Package	(CQ256), CG/LG484, CG/LG896
Total Ionizing Dose	15 to 25 krad (Si)
Single-Event Latch-Up Immunity (SEL)	LET _{TH} > 96 MeV-cm ² /mg
Single-Event Upsets (SEU) (before TMR)	LET _{TH} > 6 MeV-cm ² /mg
Supply Voltage	1.2V - 1.5V & 3.3V



CONTACT INFORMATION

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