

GRFPU

High Performance Floating Point Unit

Introduction

The GRFPU is an IEEE-754 compliant floating-point unit, supporting both single and double precision operands. The advanced design combines high throughput with low latency, providing up to 1 GFLOPS on a 45 nm ASIC process. The host interface is clean and versatile, simplifying the interfacing to processor pipelines and DSPs. The accuracy and convergence of the FPU algorithms have been proven mathematically, and the implementation has been validated with more than 20 million test vectors. Special test programs such as Testfloat, UCBTEST and IEEECC754 have been used, as well as floating-point based application software.

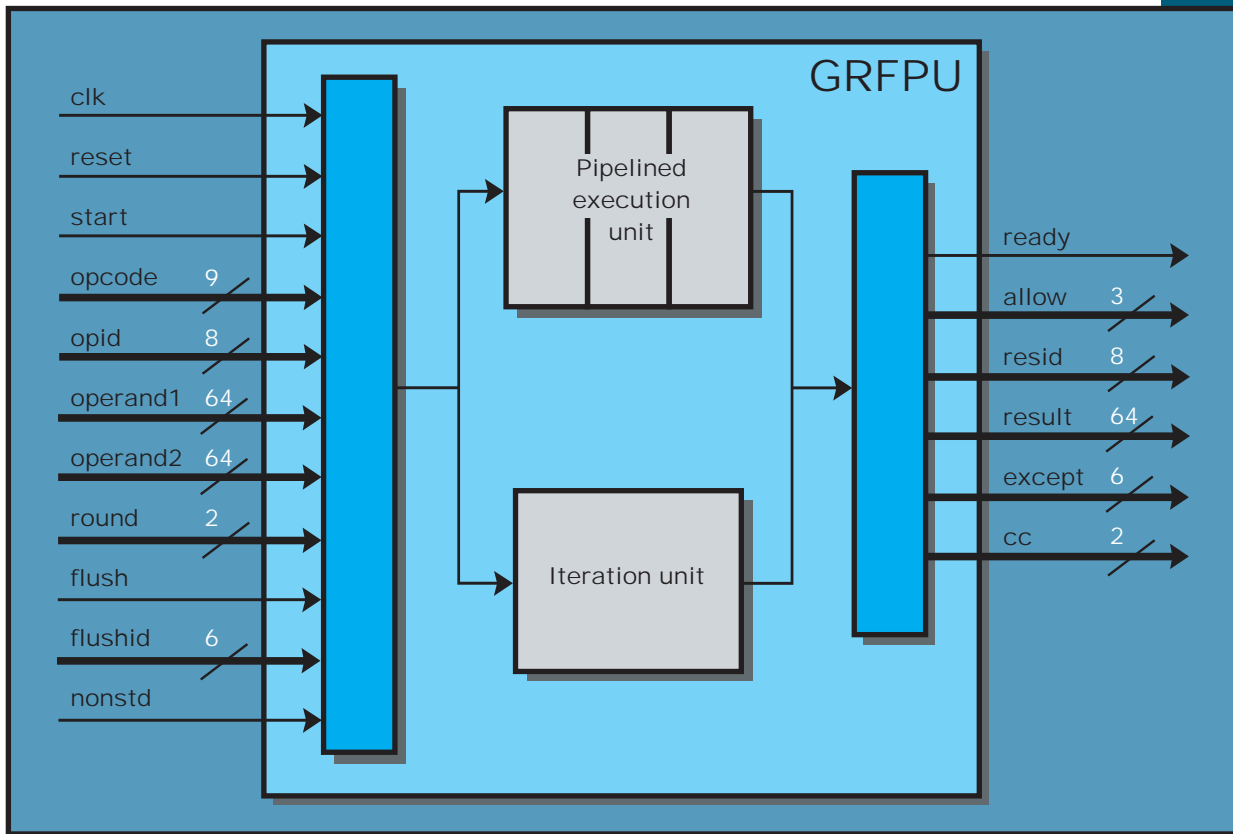


Figure 1: GRFPU block diagram

Features

- IEEE-754 compliant, supporting all rounding modes and exceptions
- Operations: add, subtract, multiply, divide, square-root, convert, compare, move, abs, negate
- Data formats: single and double precision (32- and 64-bit floats)
- Fully pipelined, 4 clock cycles latency for all operations except divide and square-root
- Non-blocking parallel execution of divide or square-root operations with other operations
- Clean and versatile interface
- LEON FPU Control unit available
- Supports all SPARC V8 floating-point instructions
- 400 MHz (400 MFLOPS) on a typical 0.13 μm standard cell process using approximately 80 kgates
- 65 MHz (65 MFLOPS) on a Virtex-II FPGA using approximately 8,500 LUTs
- Fault-tolerant (FT) version available

Functional Description

The GRFPU performs operations on single and double precision floating-point operands. All operations are IEEE-754 compliant, except for denormalized numbers that can rise exceptions or be automatically flushed to zero. The specified four rounding modes and the detection of exception conditions are fully supported. An FPU operation is started by providing the operands, opcode and rounding mode on a rising clock edge. The result and the exception flags will be available four clock cycles later. The FPU is fully pipelined and a new operation can be started every clock cycle. The only exceptions are the FDIV and FSQRT instructions which require between 16 and 25 clock cycles to complete, and which are not pipelined. Instead, they are calculated in a separate non-blocking execution unit, allowing all other operations to be performed in parallel without stalling the FPU pipeline. The table below summarises the throughput and latency of the supported operations.

Operation	Throughput	Latency	Description
FADDS, FADDD, FSUBS, BSUBD, FMULS, FMULD, FSMULD	1	4	Add, subtract, multiply
FITOS, FITOD, FSTOI, FDTOI, FSTOD, FDTOS	1	4	Convert float/integer
FCMPS, FCMPD, FCMPE, FCMPEP	1	4	Compare
FDIVS/FDIVD	16/17	16/17	Divide (single/double)
FSQRTS/FSQRTD	24/25	24/25	Square-root (single/double)

Table 1: GRFPU throughput and latency

LEON FPU Control Unit

The GRFPU can be attached to a LEON processor through the LEON FPU Control unit (GRFPC). The control unit receives SPARC FPU instructions (FPOP) from the LEON integer unit, and schedules them for execution by the FPU. The FPOPs are executed in parallel with other integer instructions, the LEON pipeline is only stalled in case of operand or resource conflicts.

The control unit also includes the FPU register file, the SPARC floating-point status register (FSR) and a deferred trap queue. For multiprocessor systems, a single GRFPU can be shared between multiple processors each with its own GRFPC. The GRFPC is available for LEON2, LEON3 and LEON4 both in a standard version and in a fault-tolerant (FT) version.

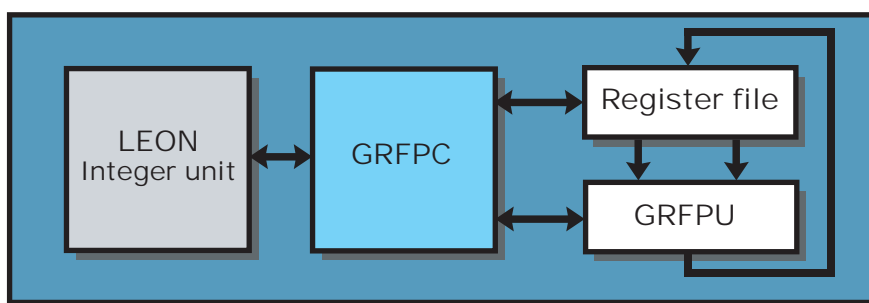


Figure 2: Block diagram of a LEON processor interface

Fault-tolerance

The fault-tolerant version of GRFPU and GRFPC includes SEU protection by design. The FPU register file is protected using 8-bit parity coding and sparing, while all other registers are optionally protected with TMR.

Availability

GRFPU and GRFPC are available in netlist format. For price and licensing conditions, please contact Aeroflex Gaisler.

CONTACT INFORMATION

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