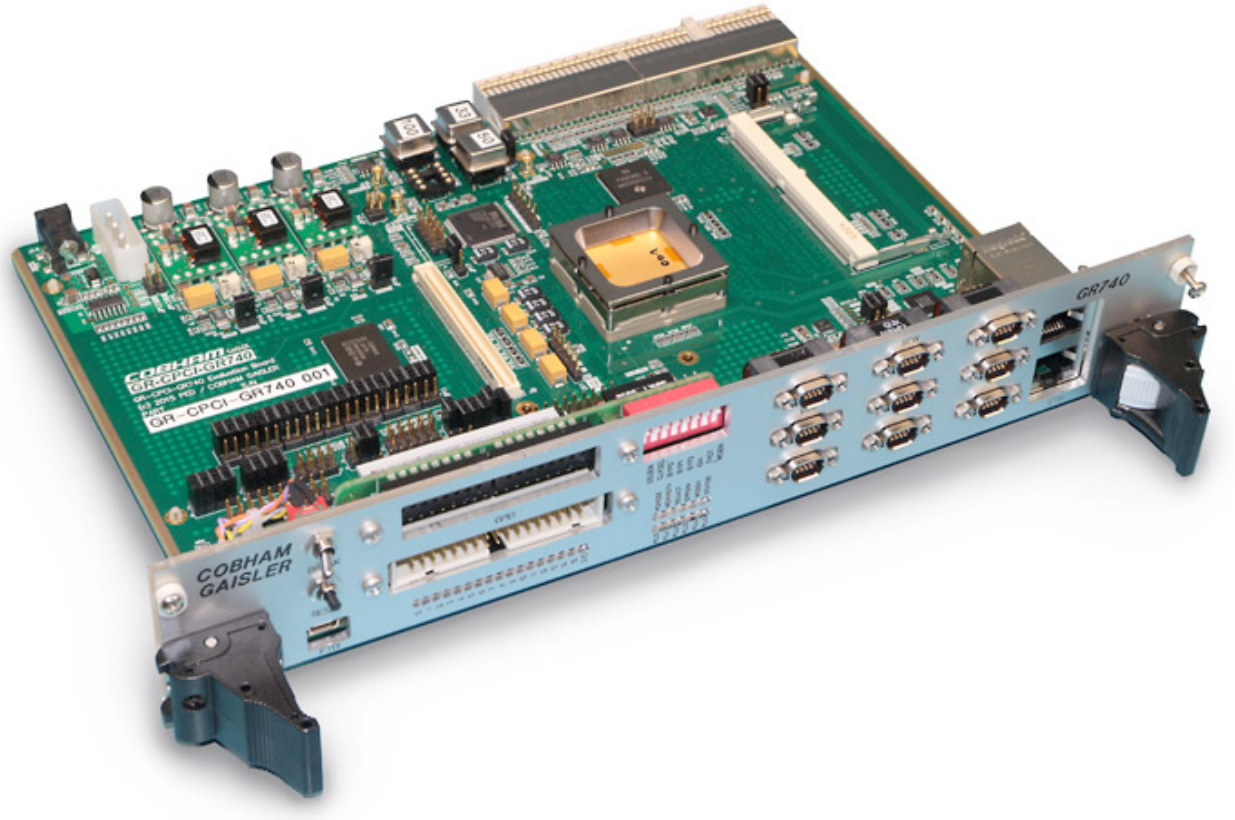
GR740 Technical Note on Benchmarking and Validation



Technical Note

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1 INTRODUCTION

1.1 Scope of the Document

This document establishes the technical note on validation and benchmarking for the NGMP engineering models (product code GR740). The GR740 work was performed in an activity initiated by the European Space Agency under ESTEC contract 2000113922/15/NL/LF.

The work has been performed by Cobham Gaisler AB, Göteborg, Sweden.

Information and additional documentation for the GR740 device is available at the product webpage: http://www.gaisler.com/gr740

1.2 Reference Documents

[UMDS] "Quad Core LEON4 SPARC V8 Processor, GR740, Data Sheet and User's Manual", Cobham Gaisler, GR740-UM-DS version 1.6, November 2016
Online: http://www.gaisler.com/gr740

[GAIA] “RTEMS SMP Executive Summary, Development Environment for Future Leon Multi-core”, RTEMSSMP-ES-001 issue 2 revision 2, March 2015 Online:
http://microelectronics.esa.int/ngmp/RTEMS-SMP-ExecSummary-CGAislerASD-OAR.pdf

[PPMSS] “Parallel Programming Models for Space Systems, Final Report”, ppm4ss-FinalReport, June 2016 Online: http://microelectronics.esa.int/ngmp/ppm4ss-FinalReport.pdf

[CMP] “Comparison between GR740, LEON4-N2X AND NGMP”, GR740-CMP, June 2015, Online: http://www.gaisler.com/doc/gr740/GR740-CMP.pdf

[SPW] Space engineering: SpaceWire - Links, nodes, routers and networks, ECSS-E-ST-50-12C, July 2008

[RMAP] Space engineering: SpaceWire - Remote memory access protocol, ECSS-E-ST-50-52C, February 2010

[SPWPNP] Space Engineering: SpaceWire Plug-and-Play protocol, ECSS-E-ST-50-54C, Draft, March 2013

[SPWD] SpaceWire-D - Deterministic Control and Data Delivery over SpaceWire Networks, Draft B, April 2010, ESA Contract Number 220774-07-NL/LvH

[BOUM] “GR-CPCI-GR740 Development Board User's Manual”, Cobham Gaisler, GR- CPCI-GR740-UM, Version 1.5, November 2016.
Online: http://www.gaisler.com/gr-cpci-gr740

[CMARK] http://www.eembc.org/coremark/, 2016-09-09

[EEMBC] http://www.eembc.org/, 2016-09-09

2 ABBREVIATIONS

AHB	Advanced High-performance Bus, part of AMBA 2.0 Specification
AMBA	Advanced Microcontroller Bus Architecture, bus architecture widely used for on-chip buses in SoC designs.
APB	Advanced Peripheral Bus, part of AMBA 2.0 Specification
ASIC	Application Specific Integrated Circuit
BCH	Bose-Hocquenghem-Chaudhuri, class of error-correcting codes
CPU	Central Processing Unit
DCL	Debug Communication Link
DMA	Direct Memory Access
DSU	Debug Support Unit
EDAC	Error Detection And Correction
EDCL	Ethernet Debug Communication Link
FLOPS	Floating Point Operations Per Second
FPU	Floating Point Unit
I/O	Input/Output
JTAG	Joint Test Action Group (developer of IEEE Standard 1149.1-1990)
KiB	Kibibyte, 2^{10} bytes, unit defined in IEEE 1541-2002
Mb, Mbit	Megabit, 10^6 bits
MB	Megabyte, 10^6 bytes
MiB	Mebibyte, 2^{20} bytes, unit defined in IEEE 1541-2002
MIPS	Million of Instructions Per Second
NGMP	Next Generation Microprocessor
OS	Operating System
PCI	Peripheral Component Interconnect
PROM	Programmable Read-Only Memory
RAM	Random Access Memory
RMAP	Remote Memory Access Protocol
RS232	Recommended Standard 232, standard for serial data signals
SDRAM	Synchronous Dynamic Random Access Memory
SEL/SEU/SET	Single Event Latchup/Upset/Transient
SPARC	Scalable Processor ARChitecture
SOC, SoC	System-On-a-Chip
TMR	Triple Modular Redundancy
UART	Universal Asynchronous Receiver/Transmitter

3 OVERVIEW

The GR740 [UMDS] is a four LEON4FT core processor built around five AMBA AHB buses. One 128-bit Processor AHB bus, one 128-bit Memory AHB bus, two 32-bit I/O AHB buses and one 32-bit Debug AHB bus. The Processor AHB connects the four LEON4FT processor cores to a shared 2 MiB L2 cache. The Memory AHB bus is located between the L2 cache and the main external memory interface (SDRAM) and attaches a memory scrubber. The two separate I/O AHB buses connect peripheral cores such as PCI master/target, PROM/IO memory controller, timers, interrupt controllers, UARTs, general purpose I/O port, SPI controller, MIL-STD-1553B interface, Ethernet MACs, CAN controllers, and a SpaceWire router. The fifth bus, a dedicated 32-bit Debug AHB bus, connects a debug support unit (DSU), that allows for non-intrusive debugging through the DSU and direct access to the complete system.

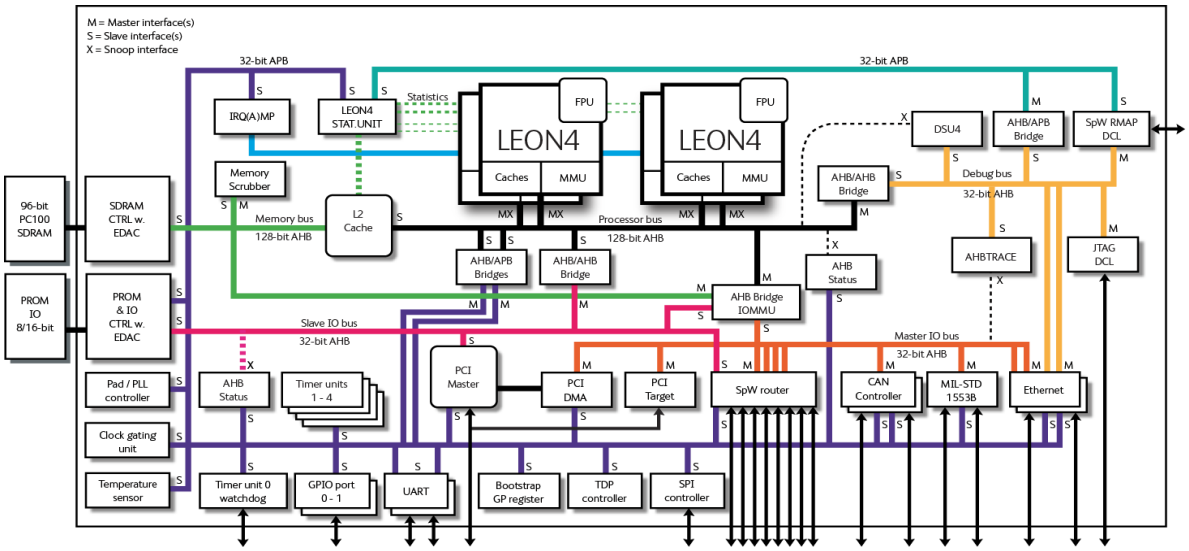

Figure 1. GR740 architecture block diagram

Following the manufacturing of the GR740 device an extensive test and validation effort has been undertaken. This technical note presents results from primarily the functional validation effort that was conducted using the GR-CPCI-GR740 [BOUM] development board (see figure 2).

More information, including user manuals for both the device and development board, can be found at the web pages:

- http://www.gaisler.com/gr740 – GR740 product page
- http://www.gaisler.com/gr-cpci-gr740 – GR-CPCI-GR740 product page

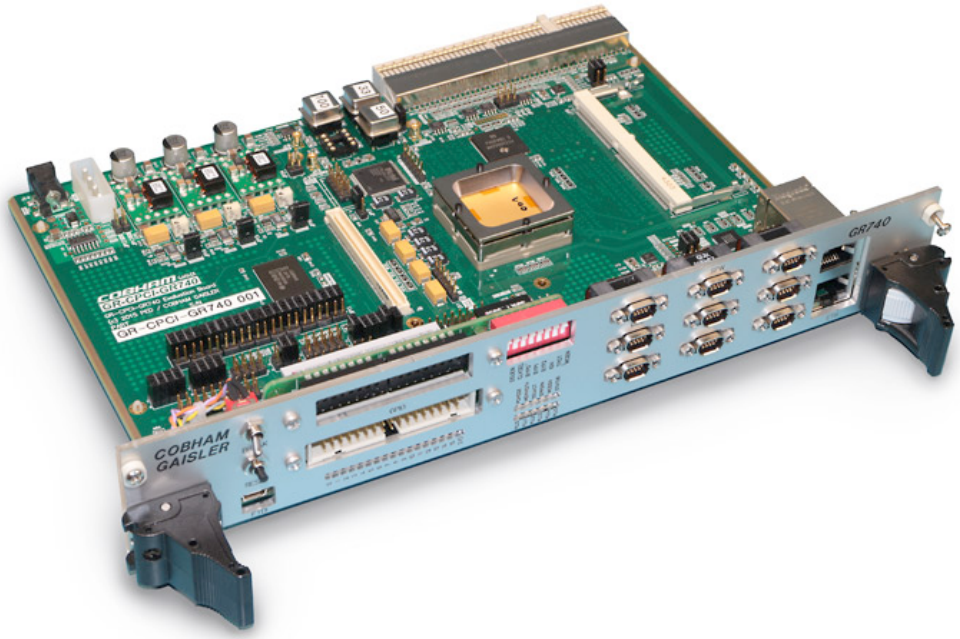

Figure 2. GR-CPCI-GR740 Development board

In addition to the benchmarking efforts performed by Cobham Gaisler there are also other evaluations that are applicable to the GR740 device. These include:

- RTEMS Multi-Core and GAIA VPU demonstrator [GAIA] – Comparison of PowerPC SCS750 and the LEON4-N2X device, which is a functional prototype of the GR740.
- Parallel Programming Models for Space Systems [PPMSS] - Evaluated the potential benefits of using the OpenMP tasking model into the space domain in terms of programmability, performance and time predictability.

Note that the GR740 device is the first rad-hard silicon that comes from the development done within the European Space Agency's Next Generation Microprocessor (NGMP) activities. During the development, several prototypes have existed and benchmark results and evaluation have been performed for these prototypes. The NGMP is an architecture that has evolved and changed over time, benchmark results obtained on prototypes may not be representative of the architecture finally implemented as the GR740. A comparison document between what was the final specification within the NGMP phase 1 activities, the functional prototype implementation (LEON4-N2X) and the first rad-hard silicon (GR740) is available in [CMP].

4 PROCESSING PERFORMANCE

4.1 Single core performance

Each LEON4FT is a SPARC V8 processor core with 7-stage pipeline, 8 register windows, 4x4 KiB instruction and 4x4 KiB data caches., MMU and a double-precision IEEE-754 FPU floating-point unit. The processor runs at 250 MHz nominal frequency, capable of executing one double precision FLOP per cycle per core. Several benchmark suites have been run on the processor:

- Each processor provides 459 Dhrystone MIPS (or DMIPS) per core , which gives 1.84 DMIPS/MHz.
- Each processor provides 200.6 Whetstone MIPS (or MWIPS), which gives 0.8 MWIP/MHz.
- The Linpack benchmark reports 22.7 MFLOPS.
- The EEMBC CoreMark 1.0 reports 511.7 CoreMarks [CMARK].
- The EEMBC Autobench 1.1 reports 111.97 AutoMarks [EEMBC].
- The EEMBC FPMark 1.3 reports 189.18 FPMarks [EEMBC].
- The EEMBC CoreMark-Pro 1.1 reports 73.48 CoreMarks [EEMBC].

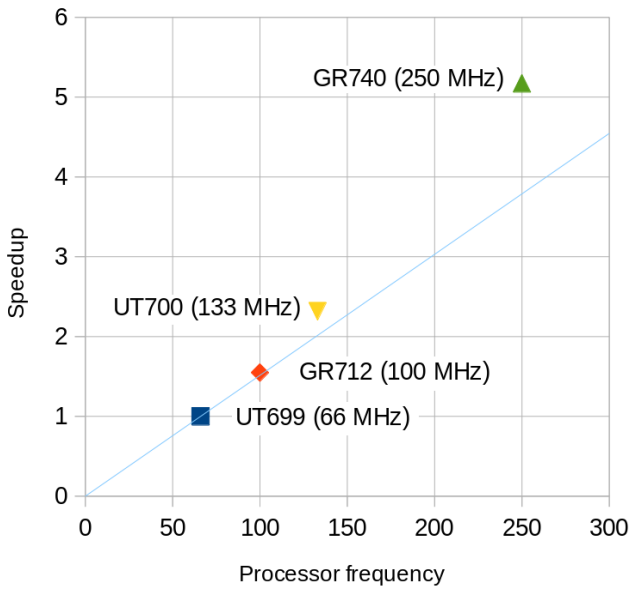

Figure 3. Cobham Gaisler device comparison (single-core)

Compared with previous generations of Cobham Gaisler devices, the GR740 provides a significant performance improvement, 5.17x with respect to the UT699, 3.36x with the GR712 and 2.24x with the UT700, as seen in the figure above. The speedup is obtained as an average improvement of a collection of benchmark figures, such as Dhrystone, Whetstone, Linpack, SPEC CPU2000 and other software applications. Please note that this result is single-core performance, which means that only one of the two cores of the GR712 and one of the four cores of the GR740 are used.

4.2 Multi core performance

The GR740 comprises four LEON4FT that can theoretically provide 4 times the single-core performance. To evaluate the multicore performance we use PARSEC 3.0 benchmarks running on top of Linux OS. PARSEC are multithreaded benchmarks, representative of shared-memory programs for multiprocessors. These benchmarks are able to obtain 3.9x which is almost the maximum theoretical speedup in a four core processor (4x).

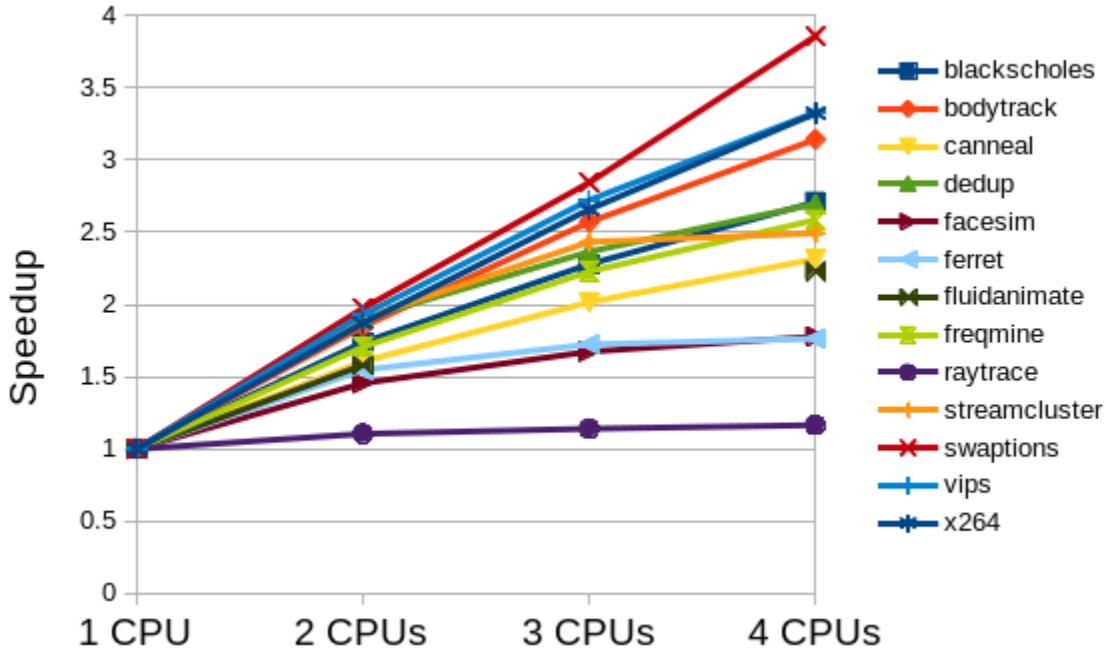

Figure 4. PARSEC 3.0 results.

We also used the EEMBC Multibench 1.1 on top of Linux OS, reporting 69.3 MultiMark, 69.3 ParallelMark and 44.4 MixMark [EEMBC].

4.3 Impact of bus interference between processors

The GR740 uses a AMBA AHB bus to connect the four LEON4FT cores to the shared 2 MiB L2 cache. When more than one core try to access the L2 cache at the same time, only one of the cores gets access to the bus and the others have to wait, therefore being interfered. This interference translates into an increase of the overall execution time of the task running on the processor.

In order to mitigate this interference, the GR740 implements an AHB bus with split transactions, which means that when a core accessing the bus is waiting for a response (such a L2 cache miss that has to go to fetch data from memory), another core can use the bus while that response becomes available. This greatly reduces the impact of bus interference and reduces the bottlenecks of parallel execution.

To illustrate the impact of split transactions, we have devised an experiment based on two microkernels: one designed to suffer the worst possible impact of interference on the bus (a.k.a. victim) and another one that generates the worst interference possible on the bus (a.k.a. interferer). We run one victim in one of the cores against 1, 2 or 3 interferers on the other cores and measure the victim's increase on execution time. The following figure clearly shows how the split transactions reduce the impact of interference, up to 3.3x times less interference in the worst-case.

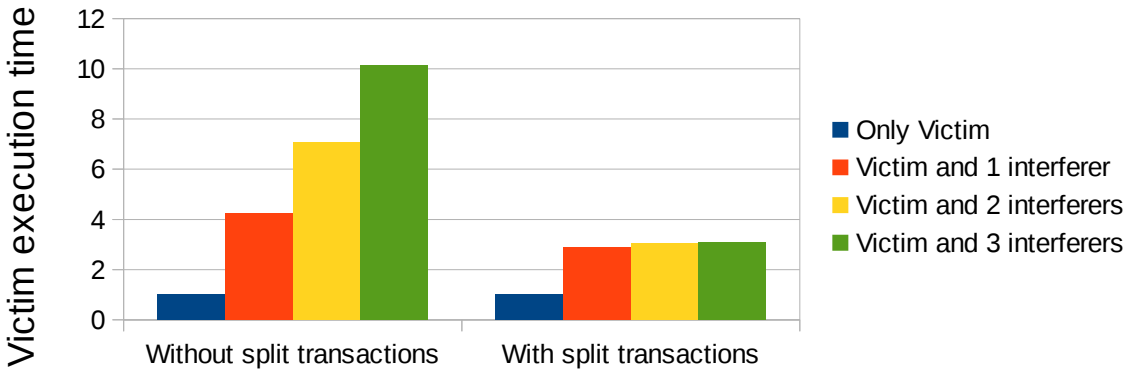

Figure 5. Impact of AMBA SPLIT transactions on bus interference

Please note that this level of interference is very unlikely to happen in real life, since these microkernels are constantly and solely using the bus (therefore constantly missing on the L1 caches). Typical software will spend most time executing from private L1 caches.

4.4 IO performance

The GR740 has a SpaceWire router with eight SpaceWire links . The router implements a routing switch, as defined in [SPW] with a RMAP target for configuration [RMAP]. Among the features supported by the router are: group adaptive routing, packet distribution, system time-distribution, distributed interrupts, port timers to recover from deadlock situations, SpaceWire-D [SPWD] packet

truncation based time-slot violations, and SpaceWire Plug-and-Play [SPWPNP]. Each SpaceWire link can operate at 400 MHz, providing an effective measured data transfer rate of 320 Mbps. The maximum measured RMAP transfer rate using 400 MHz links is 255 Mbps.

The GR740 also has a 32 bit PCI Initiator/Target interface with DMA that can achieve data transfer rates of 859 Mbps with a 33 MHz PCI clock.

The device also includes 2x 10/100/1000 Mbit Ethernet, MIL-STD-1553B interface, 2x CAN 2.0 controller interface and SPI.

5 POWER CONSUMPTION

Several power measurements have been carried out with the processor on the default configuration (processor at 250 MHz and memory at 100 MHz) and running at 50 MHz. The measurements are taken reading the available power measurement circuits on the board (via I2C) at room temperature. These measurements provide Voltage and Current of the three device supply lanes: i) 1V2 – Core supply, ii) 2V5 – IO LVDS supply and iii) 3V3 – IO supply. These values are sampled every second and the mean power consumption over time is computed on each scenario.

The different scenarios comprise the processor at reset (1), idle (2), or running different benchmarks. The Dhrystone and Coremark single-core benchmarks with LVDS signals on and off are used in scenarios 3, 4, 5 and 6. A PARSEC benchmark is run using one and four cpus in scenarios 7 and 8. The SPEC CPU2000 benchmarks are run also with one and four cpus in scenarios 9, 10, 11 and 12. All scenarios use the nominal frequency, 250 MHz, except 11 and 12 that run at 50 MHz.

Please note that no internal clock is present during the reset scenario (scenario 1) since while asserting reset the PLLs are held in power down and no clock goes into the system. Also note that the LVDS SpaceWire signals can be turned off to reduce its power consumption (roughly 200 mW).

The next scenarios, from 13 to 16, use a single-core RTEMS application to transfer data using SpaceWire at different link speeds or internally on the Spacewire router. The last scenarios, 17 and 18, run the ttcp application on top of Linux SMP using all four cpus (17) and RTEMS single-core (18). Table 1 and Figure 6 summarize results, showing the power consumption for different supplies and the total power consumed (addition of all three supply lanes):

Scenario	Description	Core Power	LVDS Power	I/O Power	Total Power
1	Processor hold at reset	42	345	166	553
2	Idle (LVDS on)	316	350	248	914
3	Dhrystone (LVDS off)	506	159	249	914
4	Dhrystone (LVDS on)	528	350	250	1128
5	Coremark (LVDS off)	523	149	254	926
6	Coremark (LVDS on)	525	350	251	1127
7	PARSEC (single core/LVDS off)	532	145	251	928
8	PARSEC (all cores/LVDS off)	1010	145	235	1391
9	CPU2000 (single core/LVDS on)	645	380	189	1213
10	CPU2000 (all cores/LVDS on)	1161	371	272	1804
11	CPU2000 (single core/LVDS on) @ 50 MHz	157	378	111	645
12	CPU2000 (all cores/LVDS on) @ 50 MHz	292	378	95	765
13	Spacewire router internal traffic (LVDS on)	620	420	268	1308
14	Spacewire 100 MHz link-rate (LVDS on)	593	429	228	1250
15	Spacewire 200 MHz link-rate (LVDS on)	603	433	273	1309
16	Spacewire 400 MHz link-rate (LVDS on)	626	449	278	1353
17	Ethernet Linux SMP (all cores/LVDS on)	1036	373	241	1649
18	Ethernet RTEMS UP (single core/LVDS on)	420	350	247	1017

Table 1: Power measurements in mW

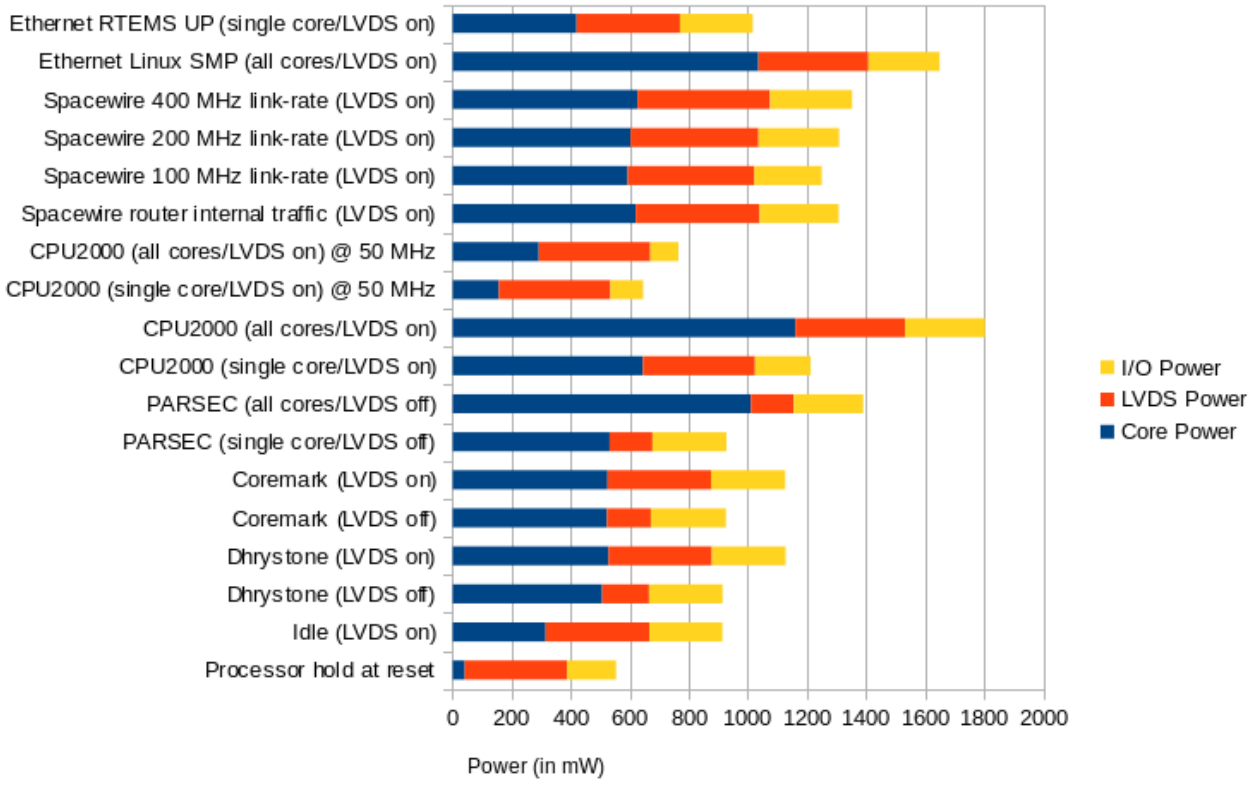

Figure 6: Power measurements in different scenarios

6 RADIATION TOLERANCE

The GR740 includes error correction schemes to tolerate radiation induced Single Event Effects. Device operation in a radiation environment has been verified through a series of Single Event Effects test campaigns with both heavy-ions and protons. As part of these tests, errata have been found in the way the Level-2 cache handles correctable tag errors and uncorrectable errors. These corner cases require additional mitigation at software level if the device is to be exposed to either heavy-ions or protons. The issues found in this first silicon have been analysed and reproduced with error injection simulations that targeted the Level-2 cache and/or the external SDRAM. A solution has been developed, possibly requiring a software reset, and the issues are planned to be corrected in a future revision of the device.

Excluding the effect of the errata mentioned above, the worst-case Single Event Effect rate estimated for a LEO-Polar orbit environment (850km, 98.7 degree inclination, AP8 min, Solar minimum, Z=1-92, Al equivalent shielding = 1g/cm2) is 1E-4 events per device and day. This results in a mean time between events, i.e. two software crashes due to uncorrectable errors, of over 27 years in actual operation. All errors are recoverable by resetting the device. In GEO and for LEO orbits with lower inclinations than polar ones the rates will be lower.

The C65SPACE technology used for this device has been experimentally confirmed to be SEL-free up to LET = 60MeV/mg/cm2 at 125°C Tj and Vdd max. TID robustness up to 300 krad (Si) has also been confirmed using test vehicles. Both SEL immunity and TID robustness are planned to be validated for the GR740 product during radiation tests of the next silicon revision.