

Comparison Between GR716A and GR716B

Application Note

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TABLE OF CONTENTS

1	Introduction.....	4
1.1	Scope of the Document	4
1.2	Reference Documents.....	4
2	Overview	5
2.1	Overview	5
2.2	Comparison	5
2.3	Changes in memory map.....	8
2.4	Changes of package body size.....	9

1 INTRODUCTION

1.1 Scope of the Document

This document presents the differences between Cobham Gaisler's revised GR716B design versus the already existing GR716A device.

The GR716B microcontroller has been developed in an activity with support from the European Space Agency under ARTES Competitiveness & Growth programme. The purpose of the work was to develop a new generation microcontroller, GR716B, based on the GR716A microcontroller.

1.2 Reference Documents

The following documents are referred as they contain relevant information:

- [RD1] GR716A Preliminary Datasheet and User's manual, Version 2.0
- [RD2] GR716B Advanced Datasheet and User's manual, Version 0.2
- [RD3] LEON-REX Instruction Set Extension, Cobham Gaisler

2 OVERVIEW

2.1 Overview

The GR716B microcontroller has been developed in an activity with support from the European Space Agency under ARTES Competitiveness & Growth programme. The purpose of this activity was to develop an improved microcontroller, GR716B, based on the GR716A microcontroller and to enrich the software ecosystem by industrialization of state-of-the-art operating systems, development and simulation tools

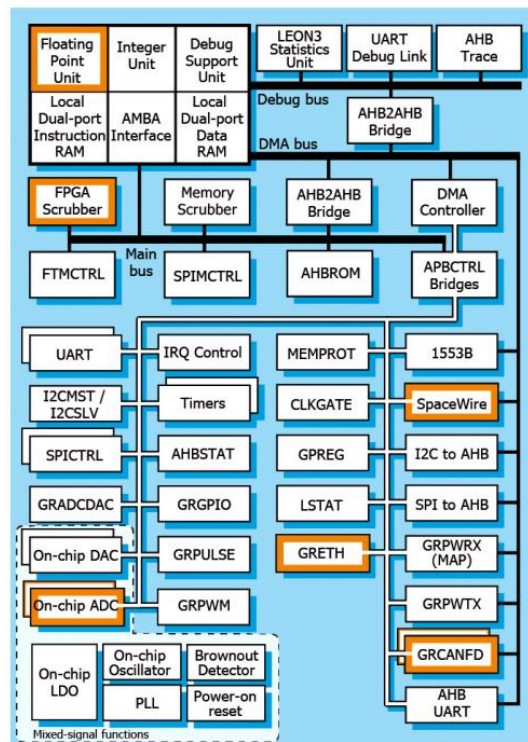


Figure 1 GR716B Block Diagram

The GR716B microcontroller is a single core LEON3FT SPARC V8 processor, with advanced interface protocols, that has been optimized for real-time systems and deterministic software execution. Features such as SPARC V8E Alternate Window Pointer, interrupt zero jitter latency, SPARC V8E multiply step instructions and the possibility to run software (including interrupt handlers) from local RAM are supported to increase the determinism and responsiveness in the system. The LEON-REX instruction set extension is also supported by the microcontroller and is further described in [RD3].

The GR716B architecture is centred around multiple instances of the AMBA Advanced High-speed Bus (AHB), to which the LEON3FT processor and other high-bandwidth units are connected. Low bandwidth peripherals/functions are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge. The use of multiple processor buses also enables non-intrusive debugging and the possibility to have direct access to on-board memory without interrupting or involving the LEON3FT processor. 64 external CMOS pins and 8 LVDS transceivers are configurable from software via configuration

registers. Pre-defined pin configurations are defined in the boot software and can be enabled by using pull-up/pull-down resistors on external pins during reset. A pre-defined configuration of external pins is useful in cases when the microcontroller should boot from external memories or remote controlled via SpaceWire, CAN FD, UART and SPI after reset. The program controlling the microcontroller needs to set appropriate direction and functionality on all pins after reset depending on the environment that the microcontroller is used in. On-chip LVDS transceivers with support for common-mode, cold-spare and fail-safe for SpaceWire and SPI for Space as well as dedicated pins for external SPI boot ROM boot are available and can optionally be used.

The microcontroller has a high level of integrated analogue functions:

- Analogue to Digital Converters (ADC)
- Brown out detection
- Crystal Oscillator
- Digital to Analogue Converters (DAC)
- Analogue Comparators
- Power-on and reset functionality
- and Linear Voltage Regulators for single 3.3V supply.

2.2 Comparison

The table below compares GR716A [RD1] and GR716B [RD2]. Differences have been marked in bold text.

Feature	GR716A	GR716B
Availability and Qualification state	Screening tests as per ESCC9000. Lot Qualification as per ESCC2567000/ESCC9000	Screening and Lot Qualification as per ESCC9000. Prototypes expected available by Q4 2022
Device ID	0x0716 / 4204	0x0716 / xxxx (TBC)
Package	CQFP132	CQFP132
Package Dimension		D2/E2 dimension is increased by 1.1 mm in the GR716B. See chapter 2.4 for more information
Power	< 200mW @ ambient room temperature < 825mW @ 110°C max power use case	< 250mW @ ambient room temperature < 1000mW @ 125°C max power use case
Supply Voltage	+3V3	+3V3
Temperature range	-55°C to +110°C	-55°C to +125°C
Radiation-tolerant	Yes	Yes
User Package Pins	Dedicated SPI memory interface 64 CMOS GPIOs with programmable pull-up / pull-down resistors 6 LVDS transceivers	Dedicated SPI memory interface 64 CMOS GPIOs with programmable pull-up / pull-down resistors, and Schmitt trigger inputs. 8 LVDS transceivers with cold-spare, fail-safe and extended common mode support. 2 LVDS transceivers are accessible via GPIO mux
Max system frequency	50MHz	100MHz
Performance	>90 DMIPS	Main CPU >180DMIPS RTA 0 >180DMIPS RTA 1 >180DMIPS
FPU	Supported	Supported by main CPU
Real Time Accelerator	n/a	Programmable Real-Time-Accelerators (RTA) improves the overall performance by a factor of 3.
Internal memory	192KiB	192KiB
External memory interface	SPI, FLASH/SRAM, I2C	SPI, FLASH/SRAM, I2C
Debug Interface	2 port UART	2 port UART
Remote access interface	SpaceWire, UART, SPI, I2C	SpaceWire, CAN FD , UART, SPI, I2C
Boot memory	SPI, FLASH/SRAM, I2C	SPI, FLASH/SRAM
SpaceWire	SpaceWire interface	SpaceWire Router with 2 external ports
CAN	CAN 2.0	CAN FD with CANOpen support

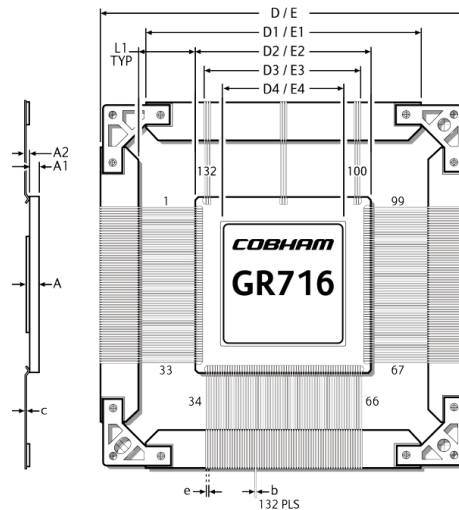
1553B	Supported	Supported
Ethernet	n/a	10/100Mbit
Hardware FPGA programming and scrubber	n/a	Support for Xilinx Virtex5 and Xilinx Kintex Ultra Scale FPGA
Misc Peripherals	UART, SPI, SPI For Space, I2C	UART, SPI, SPI For Space, I2C
PWM	Programmable PWM interface	Programmable PWM, including unique configurations for switching-power and motor-control applications.
DAC	12bit @ 3Msps, 4 channels	12bit @ 3Msps, 4 channels PWM DAC 24bit, 25Msps, 8 channels
ADC	Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended	Four ADC 11bits/14bits @ 500Ksps, 8 differential or 16 single ended
Analog comparators	n/a	20 channels, 25ns, 7 programmable internal comparison levels or external connection.
FIR Filter	n/a	8 channels, 25Msps, 27 binary programmable taps, configurable from analog comparator etc, e.g. latch-up detection applications.
DMA	Programmable DMA channels	Programmable DMA channels with support for 'if-else' statements and AES256 encryption
Analog on chip support	Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support single 3.3V supply	Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support single 3.3V supply

2.3 Changes in memory map

- General purpose register bank: The address map has been changed between the GR716A and GR716B. The functionality driven by the registers can be different between the devices due to more configurability in the GR716B device
- Analog register configuration: Address map and functionality has changed between the GR716A and GR716B
- New functionality: Configuration registers has been added for new interfaces and functions
- Support for external ADC/DAC interface has been removed

2.4 Changes of package body size

Three of the package parameters have been changed to allow new functionalities in the GR716B. Changed parameters are marked with bold text in the table below.



Name	Parameter	GR716A			GR716B		
		Min	Typ	Max	Min	Typ	Max
A			3.05	3.5		3.05	3.5
A1				2.26			2.26
A2				0.53			0.53
b1	Width of lead when closest to case	0.23		0.329	0.23		0.329
b2	Width of lead when closest to ceramic bar	0.15		0.25	0.15		0.25
c		0.075		0.175	0.075		0.175
D/E			50.85			50.85	
D1/E1			30.73			30.73	
D2/E2¹⁾		23.88		24.26	25.1		25.48
D3/E3			20.32			20.32	
D4/E4			20.2			22.0	
e			0.635			0.635	
L1¹⁾	Length of lead from case to ceramic bar (L2+L3)		8.3			7.75	
L2¹⁾	Length of lead with width b1		7.0			6.45	
L3	Length of lead with width b2		1.3			1.3	
Mass	Mass of case, including the lead frames.	8.5±1 grams			8.5±1 grams.		

Note 1 Dimension D2/E2 for GR716B is increased by 1.1 mm. To prepare PCB footprint for replacement, it is suggested to adjust the solder pad length accordingly. Dimension L1 and L2 will at the same time be reduced with by up to 0.55 mm.

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