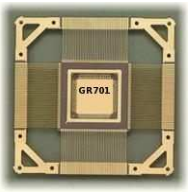
PCI to SpaceWire and 1553 Bridge
GR701A
Preliminary Data Sheet

Features

- PCI bus Initiator and Target, 32-bit, 33 MHz
- EDAC protected interface to multiple 8-bit SRAM memory, 16-bit I/O interface
- 16 kbyte EDAC protected On-chip Memory
- UARTs, Timers & Watchdog, GPIO port, Interrupt controller, Status registers
- Multiple SpaceWire links with CRC, one link with full RMAP support
- Redundant Mil-Std-1553 BC / RT / MT interface
- Redundant CAN 2.0 interface
- Up to 33 MHz system frequency
- 1.5V & 3.3V supply, 500 mW consumption

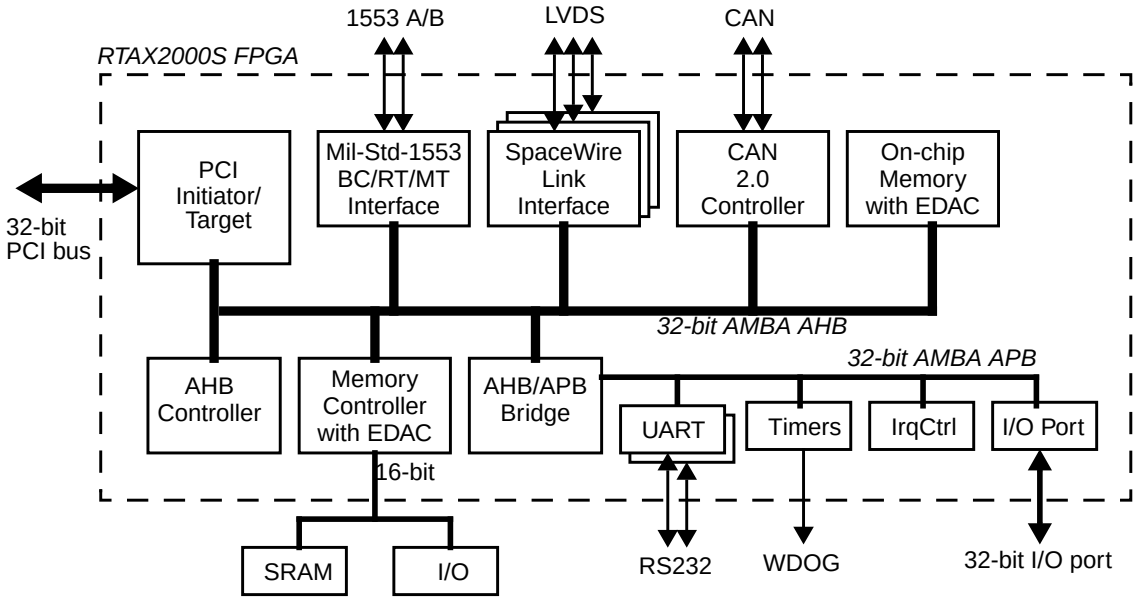
Description

GR701A is a PCI to SpaceWire and Mil-Std-1553 bridge. Its fault tolerant design is implemented using the Actel RTAX FPGA technology to enable total immunity to radiatio effects.



Specification

- CQ352 baseline package
- Total Ionizing Dose up to 300 krad (Si, functional)
- Single-Event Latch-Up Immunity (SEL) to LET_{TH} > 104 MeV-cm2/mg
- Immune to Single-Event Upsets (SEU) to LET_{TH} > 37 MeV-cm2/mg



Applications

The GR701A has been developed as a companion chip for space processors and systems with PCI interfaces. This chip is available in an Actel RTAX2000S FPGA, which makes it ideally suited for space and other high-rel applications. The chip is also available in an AX2000 FPGA for evaluation and prototyping purposes.

1 Introduction

1.1 Overview

The architecture of GR701A PCI to SpaceWire and 1553 bridge is based on the AMBA Advanced High-performance Bus (AHB), to which the high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge. The architecture is shown in figure 1.

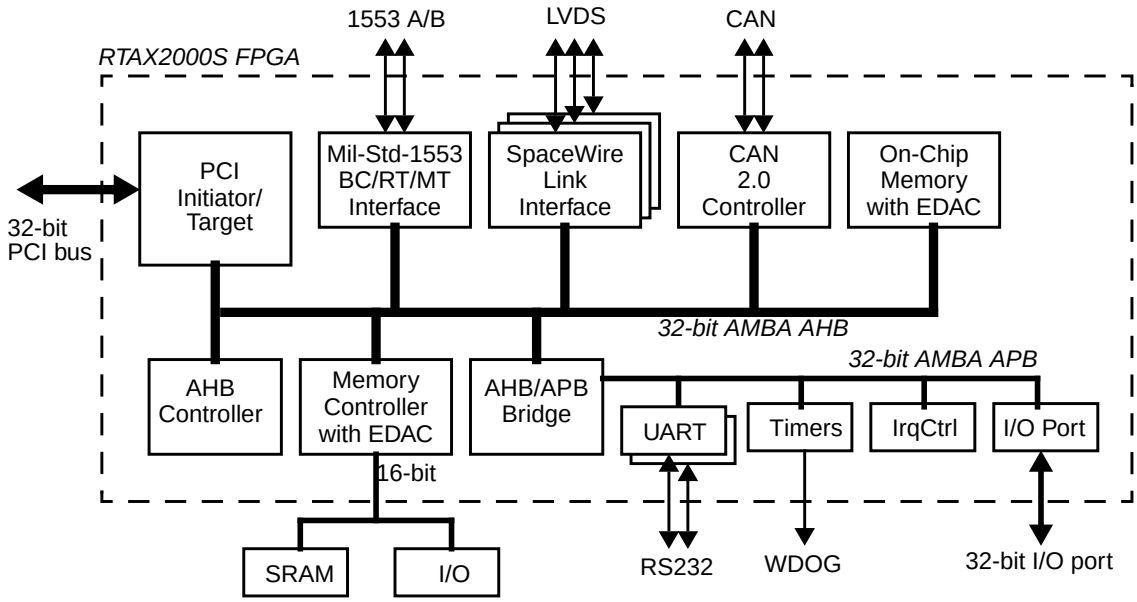


Figure 1. Architectural block diagram

The GR701A architecture includes the following modules:

- PCI bus Initiator and Target based on the Actel CorePCIF IP, 32-bit, 33 MHz
- 16 kbyte On-Chip Memory with EDAC
- 8-bit Memory Controller with EDAC for external SRAM and interface for 16-bit I/O
- Timer unit with two 32-bit timers and a watchdog
- Interrupt controller for 15 interrupts at two priority levels, forwarded to the PCI bus
- Two UARTs with FIFO and separate baud rate generators
- 32-bit general purpose I/O port (GPIO). Can also generate interrupts from external devices
- AMBA AHB status register
- Three SpaceWire links with CRC support, one link includes full RMAP support
- CAN-2.0 controller with redundant interfaces
- Mil-Std-1553 BC/RT/MT based on the Actel Core1553 IP

1.2 Signal overview

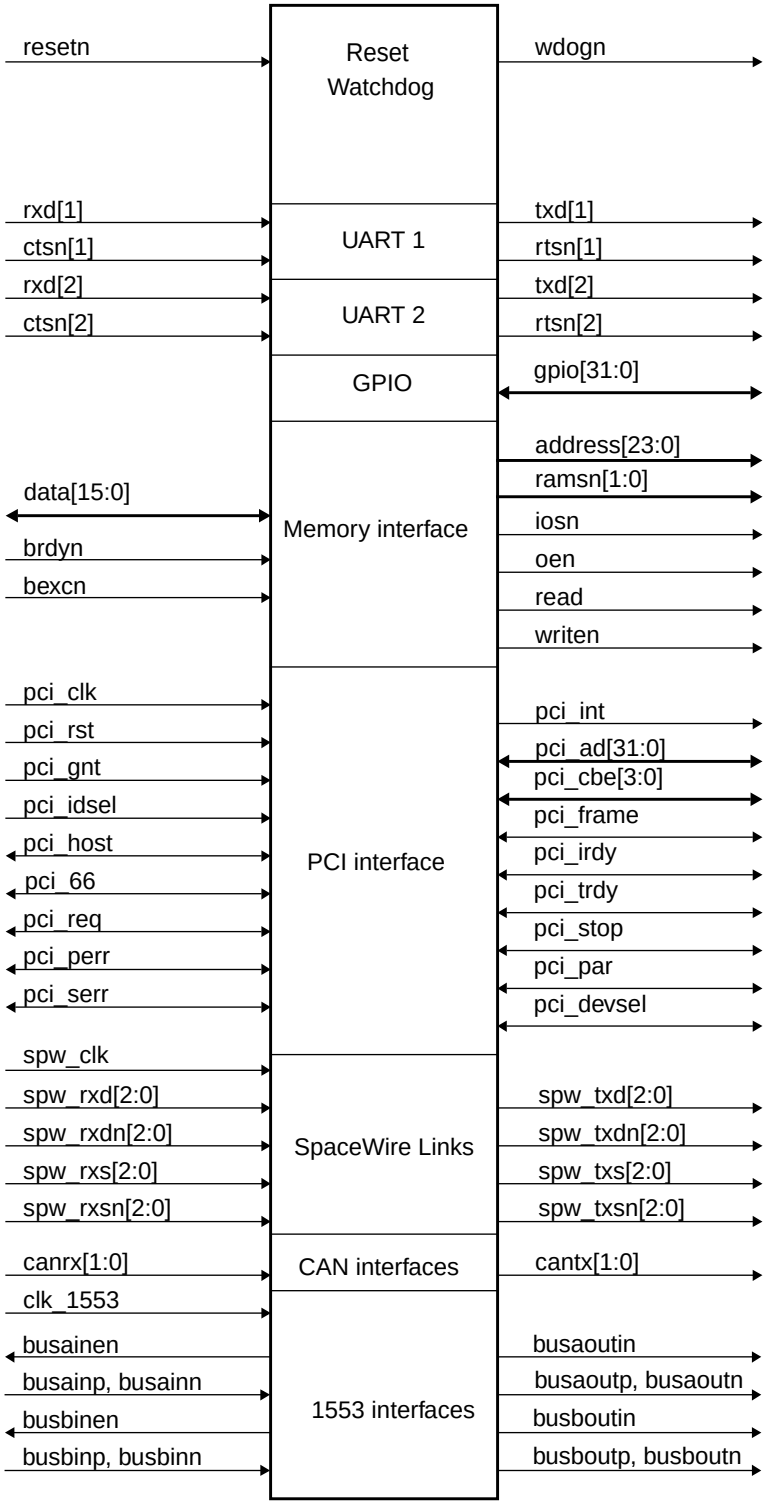


Figure 2. Signal overview

2 Architecture

2.1 Cores

The architecture of the GR701A is based on cores from the GRLIB IP library. The vendor and device identifiers for each core can be extracted from the plug & play information, as described in the user's manual. The used IP cores are listed in table 1.

Table 1. Used IP cores

Core	Function	Vendor	Device
AHBCTRL	AHB Arbiter & Decoder	0x01	-
APBCTRL	AHB/APB Bridge	0x01	0x006
PCIF	32-bit PCI interface	0x01	0x075
FTSRCTRL8	8-bit SRAM/16-bit IO Controller	0x01	0x056
FTAHBRAM	On-chip SRAM with EDAC	0x01	0x050
AHBSTAT	AHB failing address register	0x01	0x052
APBUART	8-bit UART with FIFO	0x01	0x00C
GPTIMER	Modular timer unit with watchdog	0x01	0x011
GRGPIO	General purpose I/O port	0x01	0x01A
GRSPW	SpaceWire link	0x01	0x01F
CAN_OC	CAN-2.0 interface	0x01	0x019
B1553BRM	MIL-STD-1553 BC/RT/BM	0x01	0x072

2.2 Interrupts

The GR701A uses the interrupt assignment listed in table 2. See the user's manual for how and when the interrupts are raised. All interrupts are handled by the interrupt controller and forwarded to the PCI bus.

Table 2. Interrupt assignment

Core	Interrupt	Comment
AHBSTAT	1	
APBUART 1	2	
APBUART 2	3	
CAN_OC	13	
GPTIMER	8	
GRSPW 0, 1, 2	10, 11, 12	
B1553BRM	4	
GRGPIO	1-15	Generated from external GPIO signals 1 to 15

2.3 Memory map

The memory map shown in table 3 is based on the AMBA AHB address space. Access to addresses outside the ranges will return an AHB error response. The detailed register layout is defined in the user manual.

Table 3. AMBA AHB address range

Core	Address range	Area
PCIF	0xE0000000 - 0xF0000000	PCI bus area
APBCTRL	0xFC000000 - 0xFC100000	APB bridge
FTSRCTRL8	0xFD000000 - 0xFE000000	SRAM area
	0xFE000000 - 0xFF000000	I/O area
FTAHBRAM	0xFFA00000 - 0xFFB00000	On-chip RAM
CAN_OC	0xFFFC0000 - 0xFFFC1000	Registers
B1553BRM	0xFFF00000 - 0xFFF01000	Registers
AHB plug&play	0xFFFFF000 - 0xFFFFFFFF	Registers

The control registers of most on-chip peripherals are accessible via the AHB/APB bridge, which is mapped at address 0xFC000000. The memory map shown in table 4 is based on the AMBA AHB address space.

Table 4. APB address range

Core	Address range	Comment
FTSRCTRL8	0xFC000000 - 0xFC000100	
APBUART1	0xFC000100 - 0xFC000200	
AHBSTAT	0xFC000200 - 0xFC000300	
GPTIMER	0xFC000300 - 0xFC000400	
PCIF	0xFC000400 - 0xFC000500	
FTAHBRAM	0xFC000500 - 0xFC000600	
APBUART2	0xFC000700 - 0xFC000800	
GRGPIO	0xFC000800 - 0xFC000900	
GRSPW 0	0xFC000A00 - 0xFC000B00	
GRSPW 1	0xFC000B00 - 0xFC000C00	
GRSPW 2	0xFC000C00 - 0xFC000D00	
APB plug&play	0xFC0FF000 - 0xFC100000	

2.4 Signals

The architecture has the external signals shown in table 5.

Table 5. External signals

Name	Usage	Direction	Polarity
resetn	System reset	In	Low
dsutck	JTAG Clock	In	-
dsutms	JTAG Mode	In	High
dsutdi	JTAG Input	In	High
dsutdo	JTAG Output	Out	High
address[23:0]	Memory word address	Out	High
data[15:0]	Memory data bus	BiDir	High
ramsn[1:0]	SRAM chip select	Out	Low
oen	Output enable	Out	Low
writen	Write strobe	Out	Low
read	Read cycle indicator	Out	High
iosn	I/O area chip select	Out	Low
brdyn	Bus ready	In	Low
bexcn	Bus exception	In	Low
pci_clk	PCI clock	In	-
pci_rst	PCI reset	In	Low
pci_ad[31:0]	PCI data and address	BiDir	High
pci_cbe[3:0]	PCI bus command and byte enable	BiDir	Low
pci_frame	PCI cycle frame	BiDir	Low
pci_irdy	PCI initiator ready	BiDir	Low
pci_trdy	PCI target ready	BiDir	Low
pci_stop	PCI stop	BiDir	Low
pci_par	PCI parity	BiDir	Low
pci_perr	PCI parity error	BiDir	Low
pci_serr	PCI system error	BiDir	Low
pci_idsel	PCI initialization device select	In	Low
pci_devsel	PCI device select	BiDir	Low
pci_req	PCI request	BiDir	Low
pci_gnt	PCI grant	In	Low
pci_int	PCI interrupt	Out	Low

Table 5. External signals

Name	Usage	Direction	Polarity
txd[2:1]	UART 2/1 transmit data	Out	Low
rxd[2:1]	UART 2/1 receive data	In	Low
rtsn[2:1]	UART 2/1 ready to send	Out	Low
ctsn2:[1]	UART 2/1 clear to send	In	Low
wdogn	Watchdog output	Out	Low
gpio[31:0]	General purpose I/O port (also used for SpaceWire interface configuration at reset)	BiDir	High
spw_clk	Transmitter default run-state clock	In	-
spw_rxd[2:0]	Data input, positive	In, LVDS	High
spw_rxdn[2:0]	Data input, negative	In, LVDS	Low
spw_rxs[2:0]	Strobe input, positive	In, LVDS	High
spw_rxsn[2:0]	Strobe input, negative	In, LVDS	Low
spw_txd[2:0]	Data output, positive	Out, LVDS	High
spw_txdn[2:0]	Data output, negative	Out, LVDS	Low
spw_txs[2:0]	Strobe output, positive	Out, LVDS	High
spw_txsn[2:0]	Strobe output, negative	Out, LVDS	Low
gpio[3:0]	Configuring SpaceWire start-up and default transmit rate at reset. “0000” corresponds to *spw_clk* frequency divided by 1. “0001” corresponds to the *spw_clk* frequency divided by 2, etc.	In	-
cantx[1:0]	CAN transmit data	Out	Low
canrx[1:0]	CAN receive data	In	Low
clk_1553	Clock for MIL-STD-1553 BC/RT/BM	In	-
busainen	Enable for the A receiver	Out	High
busainp	Positive data input from the A receiver	In	High
busainn	Negative data input from the A receiver	In	Low
busbinen	Enable for the B receiver	Out	High
busbinp	Positive data to the B receiver	In	High
busbinn	Negative data to the B receiver	In	Low
busaoutin	Inhibit for the A transmitter	Out	High
busaoutp	Positive data to the A transmitter	Out	High
busaoutn	Negative data to the A transmitter	Out	Low
busboutin	Inhibit for the B transmitter	Out	High
busboutp	Positive output to the B transmitter	Out	High
busboutn	Negative output to the B transmitter	Out	Low

3 PCI Initiator/Target

3.1 Overview

This core provides a complete interface to an external PCI bus, with both initiator and target functions. The interface is based on the Actel CorePCIF IP and provides an AMBA bus backend. It also provides a interrupt controller that forwards all interrupts generated on the AMBA bus to the PCI bus.

3.2 Signal definitions and reset values

The signals and their reset values are described in table 6.

Table 6. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
pci_clk	Input	PCI clock	-	-
pci_rst	Input	Reset	Low	-
pci_gnt	Input	Grant signal	Low	-
pci_idsel	Input	Device select during configuration	High	-
pci_ad[31:0]	Input/Output	Address and Data bus	High	Tri.state
pci_cbe[3:0]	Input/Output	Bus command and byte enable	Low	Tri-state
pci_par	Input/Output	Parity signal	High	Tri-state
pci_frame	Input/Output	Cycle frame	Low	Tri-state
pci_devsel	Input/Output	Device select	Low	Tri-state
pci_irdy	Input/Output	Initiator ready	Low	Tri-state
pci_trdy	Input/Output	Target ready	Low	Tri-state
pci_stop	Input/Output	Stop	Low	Tri-state
pci_perr	Input/Output	Parity error	Low	Tri-state
pci_serr	Input/Output	System error	Low	Tri-state
pci_req	Output	Request signal	Low	Logical 1
pci_int	Output	Interrupt signal	Low	Logical 1

3.3 Timing

The timing waveforms and timing parameters are shown in figure 3 and are defined in table 7.

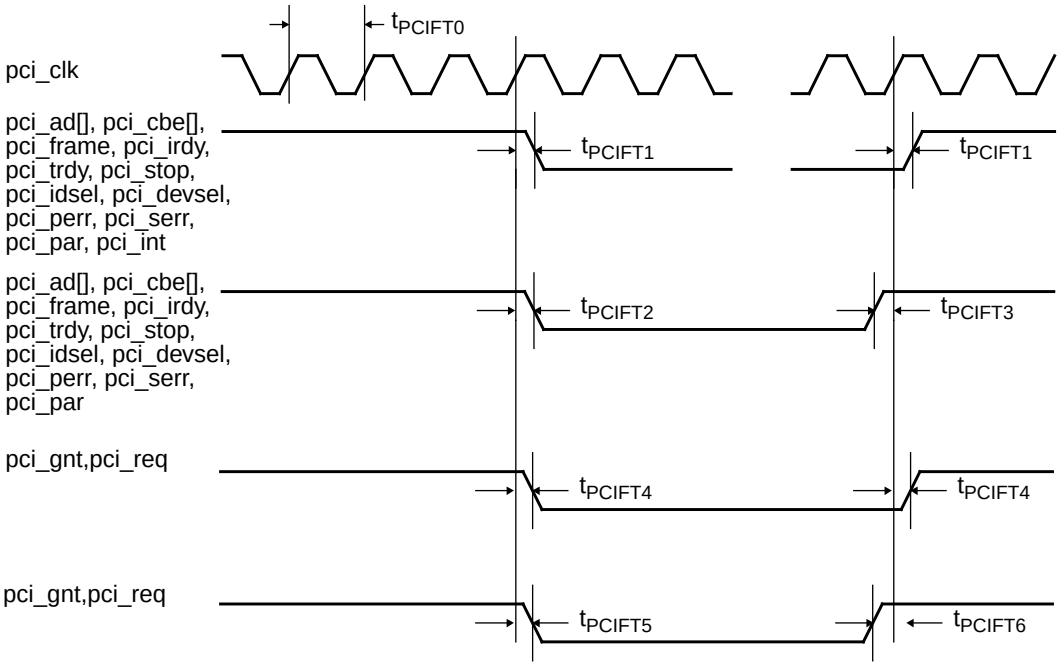


Figure 3. Timing waveforms

Table 7. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{PCIFT0}	pci clock period	-	30 *1)*	-	ns
t_{PCIFT1}	clock to output delay	rising *pci_clk* edge	2	11	ns
t_{PCIFT2}	input to clock hold	rising *pci_clk* edge	0	-	ns
t_{PCIFT3}	input to clock setup	rising *pci_clk* edge	7	-	ns
t_{PCIFT4}	clock to output delay	rising *pci_clk* edge	2	12	ns
t_{PCIFT5}	input to clock hold	rising *pci_clk* edge	0	-	ns
t_{PCIFT6}	input to clock setup	rising *pci_clk* edge	10, 12	-	ns

Note 1: The minimum clock period, and the resulting maximum clock frequency, is dependent on the manufacturing lot for the Actel RTAX2000S parts and expected radiation levels.

The degradation criterion for Propagation Delays for the RTAX2000S parts is according to Actel Total Ionizing Does Test Report 10% at 300 krad (Si). The above specified timing values are guaranteed up to 50 krad (Si). If a higher total ionizing does is expected than 50 krad (Si), the corresponding post-annealing propagation delays that can be found in the Actel Total Ionizing Does Test Report can be used to degrade the timing more accurately (typical degradation is within 1% after 300 krad (Si)).

The functional behavior of the part is guaranteed up to 300 krad (Si).

4 Memory Interface with EDAC

4.1 Overview

The fault tolerant 8-bit SRAM/16-bit I/O memory interface uses a common 16-bit data bus to interface 8-bit SRAM and 16-bit I/O devices. It provides an Error Detection And Correction unit (EDAC), correcting up to two errors and detecting up to four errors in a data byte. The EDAC eight checkbits are stored in parallel with the 8-bit data in SRAM memory. Configuration of the memory controller functions is performed through the APB bus interface.

4.2 Signal definitions and reset values

The signals and their reset values are described in table 8.

Table 8. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
address[23:0]	Output	Memory address	High	Undefined
data[15:0]	Input/Output	Memory data	High	Tri-state
ramsn[1:0]	Output	SRAM chip select	Low	Logical 1
ramoen[1:0]	Output	SRAM output enable	Low	Logical 1
oen	Output	Output enable	Low	Logical 1
writen	Output	Write strobe	Low	Logical 1
read	Output	Read strobe	High	Logical 1
iosn	Output	IO area chip select	Low	Logical 1
brdyn	Input	Bus ready. Extends accesses to the IO area.	Low	-
bexcn	Input	Bus exception.	Low	-

4.3 Timing

The timing waveforms and timing parameters are shown in figure 4 and are defined in table 9.

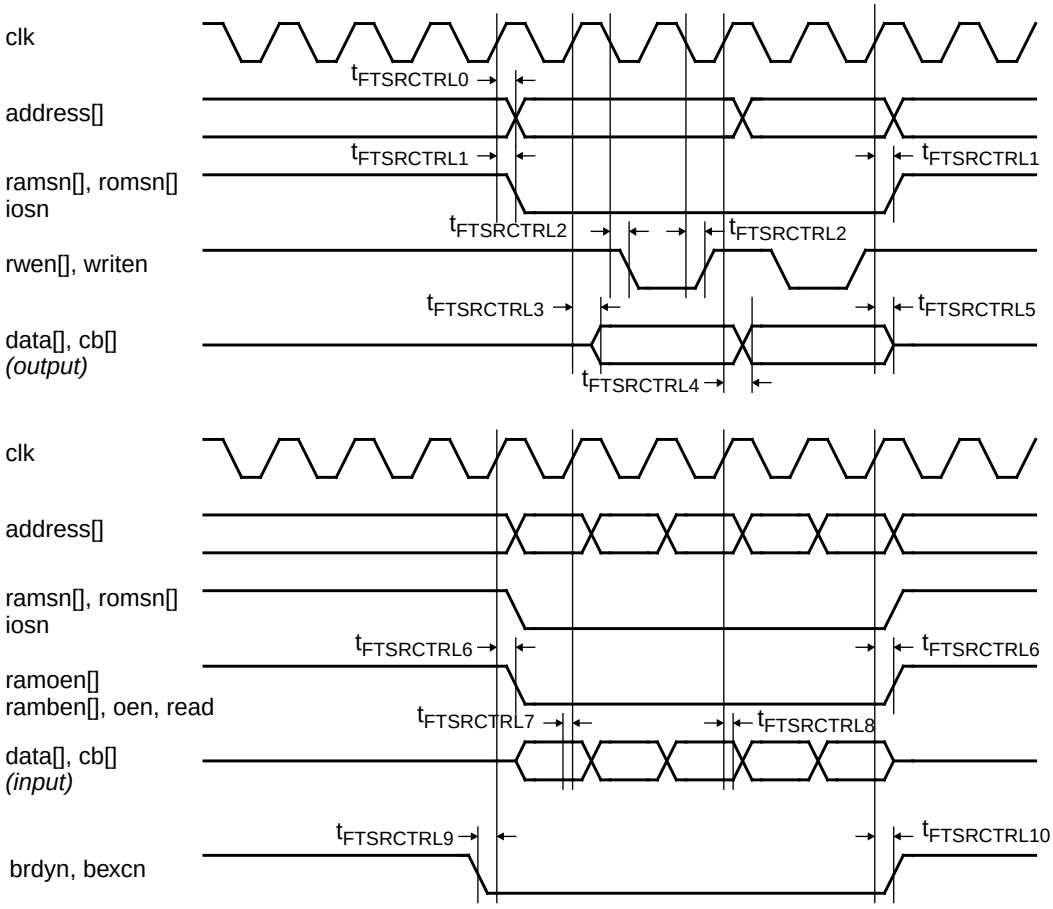


Figure 4. Timing waveforms

Table 9. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{FTSRCTRL0}$	address clock to output delay	rising clk edge	0	10	ns
$t_{FTSRCTRL1}$	clock to output delay	rising clk edge	0	10	ns
$t_{FTSRCTRL2}$	clock to data output delay	rising clk edge	0	10	ns
$t_{FTSRCTRL3}$	clock to output delay	falling clk edge	0	10	ns
$t_{FTSRCTRL4}$	clock to data non-tri-state delay	rising clk edge	0	15	ns
$t_{FTSRCTRL5}$	clock to data tri-state delay	rising clk edge	0	15	ns
$t_{FTSRCTRL6}$	clock to output delay	rising clk edge	0	15	ns
$t_{FTSRCTRL7}$	data input to clock setup	rising clk edge	7	-	ns
$t_{FTSRCTRL8}$	data input from clock hold	rising clk edge	1	-	ns
$t_{FTSRCTRL9}$	input to clock setup	rising clk edge	7	-	ns
$t_{FTSRCTRL10}$	input from clock hold	rising clk edge	1	-	ns

5 On-chip Memory with EDAC Protection

5.1 Overview

The on-chip memory is accessed via an AMBA AHB slave interface. The memory implements 16 kbytes of data. Registers are accessed via an AMB APB interface.

The on-chip memory implements volatile memory that is protected by means of Error Detection And Correction (EDAC). One error can be corrected and two errors can be detected, which is performed by using a (32, 7) BCH code. Some of the optional features available are single error counter, diagnostic reads and writes. Configuration is performed via a configuration register.

6 SpaceWire Interface

6.1 Overview

The SpaceWire core provides an interface between the AHB bus and a SpaceWire network. It implements the SpaceWire standard (ECSS-E-50-12A) with the protocol identification extension (ECSS-E-50-11).

6.2 Signal definitions and reset values

The signals and their reset values are described in table 10.

Table 10. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
spw_clk	Input	Transmitter default run-state clock	Rising edge	-
spw_rxd	Input, LVDS	Data input, positive	High	-
spw_rxdn	Input, LVDS	Data input, negative	Low	-
spw_rxs	Input, LVDS	Strobe input, positive	High	-
spw_rxsn	Input, LVDS	Strobe input, negative	Low	-
spw_txd	Output, LVDS	Data output, positive	High	Logical 0
spw_txdn	Output, LVDS	Data output, negative	Low	Logical 1
spw_txs	Output, LVDS	Strobe output, positive	High	Logical 0
spw_txsn	Output, LVDS	Strobe output, negative	Low	Logical 1

6.3 Timing

The timing waveforms and timing parameters are shown in figure 5 and are defined in table 11.

The SpaceWire jitter and skew timing waveforms and timing parameters are shown in figure 6 and are defined in table 12.

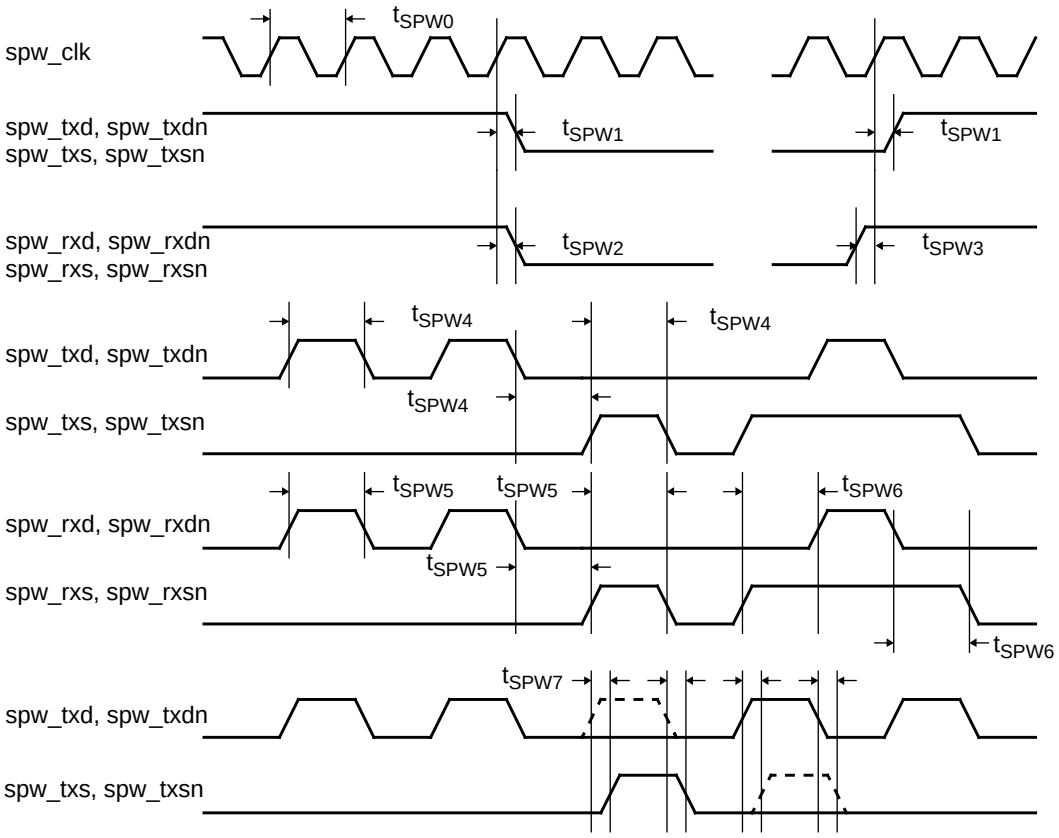


Figure 5. Timing waveforms

Table 11. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPW0}	transmit clock period	-	-	20	ns
t_{SPW1}	clock to output delay	rising *spw_clk* edge	0	20	ns
t_{SPW2}	input to clock hold	-	-	-	not applicable
t_{SPW3}	input to clock setup	-	-	-	not applicable
t_{SPW4}	output data bit period	-	-		*clk* periods
		-	t_{SPW0} -5	tSPW0 +5	ns
t_{SPW5}	input data bit period	-	20	-	ns
t_{SPW6}	data & strobe edge separation	-	10	-	ns
t_{SPW7}	data & strobe output skew	-	-	5	ns

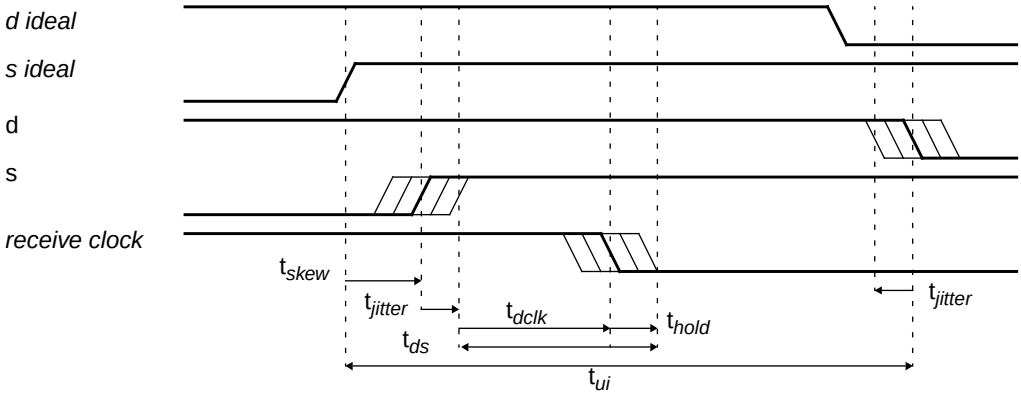


Figure 6. Skew and jitter timing waveforms

Table 12. Skew and jitter timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{skew}	skew between data and strobe	-	-	TBD	ns
t_{jitter}	jitter on data or strobe	-	-	TBD	ns
t_{ds}	minimum separation between data and strobe edges	-	TBD	-	ns
t_{dclk}	delay from edge of data or strobe to the receiver flip-flop	-	-	TBD	ns
t_{hold}	hold timer on receiver flip-flop	-	TBD	-	ns
t_{ui}	unit interval (bit period)	-	TBD	-	ns

7 MIL-STD-1553B Bus Controller / Remote Terminal / Monitor Terminal

7.1 Overview

The interface provides a complete Mil-Std-1553B Bus Controller (BC), Remote Terminal (RT) or Monitor Terminal (MT). The interface connects to the MIL-STD-1553B bus through external transceivers and transformers. The interface is based on the Actel Core1553BRM core.

7.2 Signal definitions and reset values

The signals and their reset values are described in table 13.

Table 13. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
clk_1553	Input	1553 clock signal	-	-
busainen	Output	Enable for the A receiver	High	Logical 0
busainp	Input	Positive data input from the A receiver	High	-
busainn	Input	Negative data input from the A receiver	Low	-
busbinen	Output	Enable for the B receiver	High	Logical 0
busbinp	Input	Positive data to the B receiver	High	-
busbinn	Input	Negative data to the B receiver	Low	-
busaoutin	Output	Inhibit for the A transmitter	High	Logical 0
busaoutp	Output	Positive data to the A transmitter	High	Logical 0
busaoutn	Output	Negative data to the A transmitter	Low	Logical 1
busboutin	Output	Inhibit for the B transmitter	High	Logical 0
busboutp	Output	Positive output to the B transmitter	High	Logical 0
busboutn	Output	Negative output to the B transmitter	Low	Logical 1

7.3 Timing

The timing waveforms and timing parameters are shown in figure 7 and are defined in table 14.

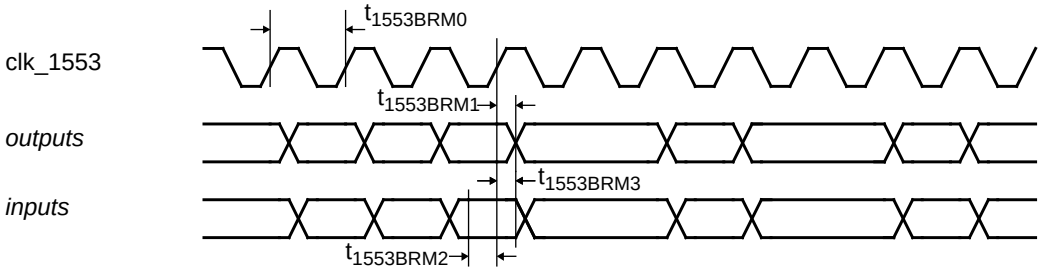


Figure 7. Timing waveforms

Table 14. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{1553BRM0}$	clock period[1)]	-	41.66	41.66	ns
$t_{1553BRM1}$	clock to data output delay	rising *clk_1553* edge	-	20	ns
$t_{1553BRM2}$	data input to clock setup	rising *clk_1553* edge	7	-	ns
$t_{1553BRM3}$	data input from clock hold	rising *clk_1553* edge	1	-	ns

Note 1: The minimum clock period, and the resulting maximum clock frequency, is dependent on the manufacturing lot for the Actel RTAX2000S parts and expected radiation levels.

The degradation criterion for Propagation Delays for the RTAX2000S parts is according to Actel Total Ionizing Does Test Report 10% at 300 krad (Si). The above specified timing values are guaranteed up to 50 krad (Si). If a higher total ionizing does is expected than 50 krad (Si), the corresponding post-annealing propagation delays that can be found in the Actel Total Ionizing Does Test Report can be used to degrade the timing more accurately (typical degradation is within 1% after 300 krad (Si)).

The functional behavior of the part is guaranteed up to 300 krad (Si).

8 CAN 2.0 Interface

8.1 Overview

This CAN interface implements the CAN 20.A and 2.0B protocolos. It is based on the Philips SJA1000 and has a compatible register map with a few exceptions.

8.2 Signal definitions and reset values

The signals and their reset values are described in table 15.

Table 15. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
cantx[]	Output	CAN transmit data	Low	Logical 1
canen[]	Output	CAN transmit enabel	-	Logical 0
canrx[]	Input	CAN receive data	Low	-

8.3 Timing

The timing waveforms and timing parameters are shown in figure 8 and are defined in table 16.

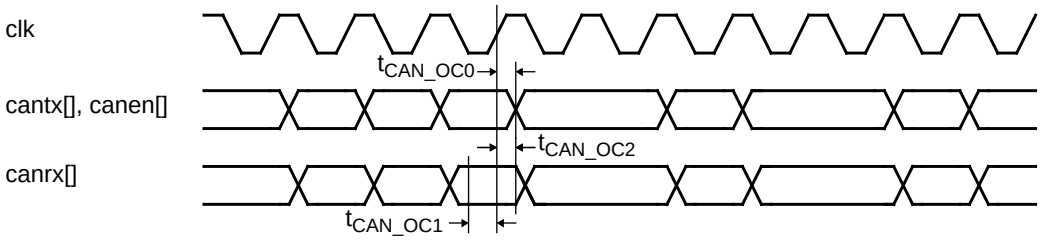


Figure 8. Timing waveforms

Table 16. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{CAN_OC0}	clock to data output delay	rising *clk* edge	0	20	ns
t_{CAN_OC1}	data input to clock setup	rising *clk* edge	-	-	ns
t_{CAN_OC2}	data input from clock hold	rising *clk* edge	-	-	ns

Note: The *canrx[]* input is re-synchronized internally. The signal does not have to meet any setup or hold requirements.

9 UART Serial Interface

9.1 Overview

The interface is provided for serial communications. The UART supports data frames with 8 data bits, one optional parity bit and one stop bit. To generate the bit-rate, each UART has a programmable 12-bit clock divider.

9.2 Signal definitions and reset values

The signals and their reset values are described in table 17.

Table 17. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
txd[]	Output	UART transmit data line	-	Logical 1
rtsn[]	Output	Ready To Send	Low	Logical 1
rxd[]	Input	UART receive data line	-	-
ctsn[]	Input	Clear To Send	Low	-

9.3 Timing

The timing waveforms and timing parameters are shown in figure 9 and are defined in table 18.

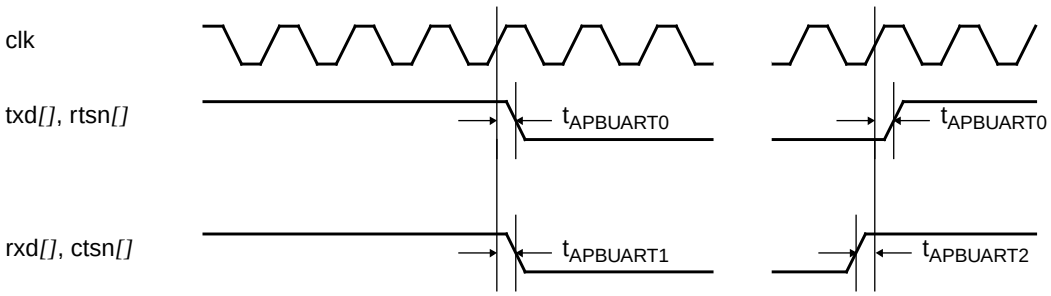


Figure 9. Timing waveforms

Table 18. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{APBUART0}$	clock to output delay	rising *clk* edge	0	20	ns
$t_{APBUART1}$	input to clock hold	rising *clk* edge	-	-	ns
$t_{APBUART2}$	input to clock setup	rising *clk* edge	-	-	ns

Note: The *ctsn[]* and *rxd[]* inputs are re-synchronized internally. These signals do not have to meet any setup or hold requirements.

10 General Purpose Timer Unit

10.1 Overview

The General Purpose Timer Unit provides a common prescaler and decrementing timer(s). The unit implements one 8 bit prescaler and 2 decrementing 32 bit timer(s). The unit is capable of asserting interrupt on timer(s) underflow.

10.2 Signal definitions and reset values

The signals and their reset values are described in table 19.

Table 19. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
wdogn	Tri-state output	Watchdog output. Equivalent to interrupt pending bit of last timer.	Low	Tri-state

10.3 Timing

The timing waveforms and timing parameters are shown in figure 10 and are defined in table 20.

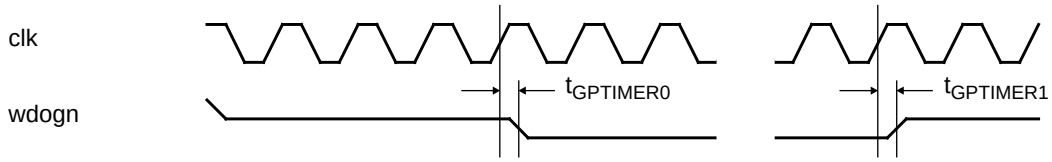


Figure 10. Timing waveforms

Table 20. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GPTIMER0}$	clock to output delay	rising *clk* edge	0	20	ns
$t_{GPTIMER1}$	clock to output tri-state	rising *clk* edge	0	25	ns

11 General Purpose I/O Port

11.1 Overview

Each bit in the general purpose input output port can be individually set to input or output, and can optionally generate an interrupt. For interrupt generation, the input can be filtered for polarity and level/edge detection.

11.2 Signal definitions and reset values

The signals and their reset values are described in table 21.

Table 21. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
gpio[]	Input/Output	General purpose input output	-	Tri-state

11.3 Timing

The timing waveforms and timing parameters are shown in figure 11 and are defined in table 22.

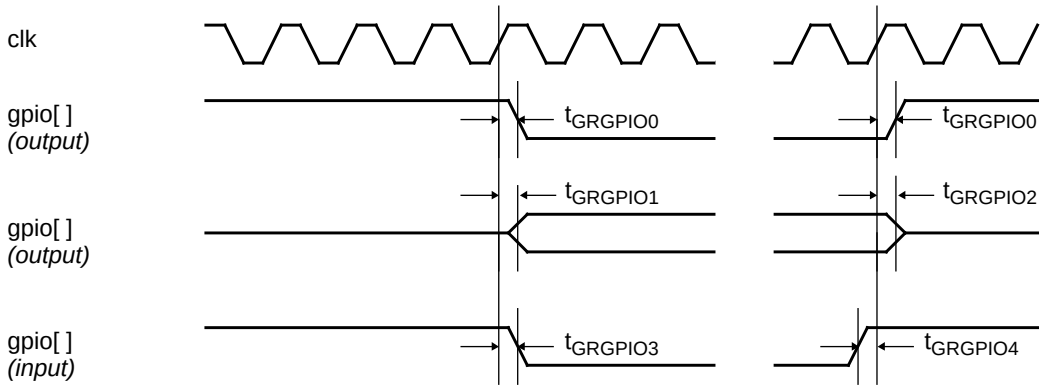


Figure 11. Timing waveforms

Table 22. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRGPIO0}$	clock to output delay	rising *clk* edge	0	20	ns
$t_{GRGPIO1}$	clock to non-tri-state delay	rising *clk* edge	0	20	ns
$t_{GRGPIO2}$	clock to tri-state delay	rising *clk* edge	0	25	ns
$t_{GRGPIO3}$	input to clock hold	rising *clk* edge	-	-	ns
$t_{GRGPIO4}$	input to clock setup	rising *clk* edge	-	-	ns

Note: The *gpio* inputs are re-synchronized internally. The signals do not have to meet any setup or hold requirements.

12 Status Registers

12.1 Overview

The status registers store information about AMBA AHB accesses triggering an error response. There is a status register and a failing address register capturing the control and address signal values of a failing AMBA bus transaction, or the occurence of a correctable error being signaled from a fault tolerant core.

13 AMBA AHB controller with plug&play support

13.1 Overview

The AMBA AHB controller is a combined AHB arbiter, bus multiplexer and slave decoder according to the AMBA 2.0 standard.

In round-robin mode, priority is rotated one step after each AHB transfer. If no master requests the bus, the last owner will be granted (bus parking).

14 AMBA AHB/APB bridge with plug&play support

14.1 Overview

The AMBA AHB/APB bridge is a APB bus master according the AMBA 2.0 standard.

15 Reset generation

15.1 Overview

The reset generator implements input reset signal synchronization with glitch filtering and generates the internal reset signal. The input reset signal can be asynchronous.

15.2 Signal definitions and reset values

The signals and their reset values are described in table 23.

Table 23. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
resetn	Input	Reset	Low	

15.3 Timing

The timing waveforms and timing parameters are shown in figure 12 and are defined in table 24.

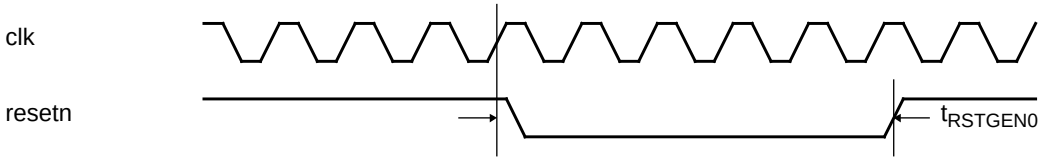


Figure 12. Timing waveforms

Table 24. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{RSTGEN0}$	asserted period	-	100	-	ns

Note: The *resetn* input is re-synchronized internally. The signals does not have to meet any setup or hold requirements.

16 Electrical description

16.1 Absolute maximum ratings

According to Actel data sheet [RTAX].

16.2 Operating conditions

According to Actel data sheet [RTAX].

16.3 Input voltages, leakage currents and capacitances

According to Actel data sheet [RTAX].

16.4 Output voltages, leakage currents and capacitances

According to Actel data sheet [RTAX].

16.5 Clock Input voltages, leakage currents and capacitances

According to Actel data sheet [RTAX].

16.6 Power supplies

According to Actel data sheet [RTAX].

17 Mechanical description

17.1 Component and package

The GR701A is implemented in the ACTEL RTAX2000S FPGA with the CQ352 package, as per Actel data sheet [RTAX] and [PACK].

17.2 Pin assignment

Table 25. Pin assignment

Name	I/O	Pin CQ352	Pin CG624	Level	Volt.	Slew	Drive	Pull	Pol-arity	Note
resetn	in	306	D24	LVTTL	3.3	-	-	None	low	Reset
dsutx	out	-	F23	LVTTL	3.3	Low	12	None	low	DSU data transmit {reserved}
dsurx	in	-	E23	LVTTL	3.3	-	-	None	low	DSU data receive {reserved}
dsutck	in	-	V6	LVTTL	3.3	-	-	None	-	DSU JTAG clock {reserved}
dsutms	in	-	W3	LVTTL	3.3	-	-	None	high	DSU JTAG mode {reserved}
dsutdi	in	-	AB2	LVTTL	3.3	-	-	None	high	DSU JTAG input {reserved}
dsutdo	out	-	AA2	LVTTL	3.3	Low	12	None	high	DSU JTAG output {reserved}
dsutck	in	4	-	LVCMOS	2.5	-	-	None	-	DSU JTAG clock {reserved}
dsutms	in	5	-	LVCMOS	2.5	-	-	None	high	DSU JTAG mode {reserved}
dsutdi	in	6	-	LVCMOS	2.5	-	-	None	high	DSU JTAG input {reserved}
dsutdo	out	7	-	LVCMOS	2.5	Low	12	None	high	DSU JTAG output {reserved}
address[0]	out	247	P9	LVTTL	3.3	High	24	None	high	Address, LSB
address[1]	out	248	N6	LVTTL	3.3	High	24	None	high	
address[2]	out	249	M6	LVTTL	3.3	High	24	None	high	
address[3]	out	250	N8	LVTTL	3.3	High	24	None	high	
address[4]	out	253	N7	LVTTL	3.3	High	24	None	high	
address[5]	out	254	M4	LVTTL	3.3	High	24	None	high	
address[6]	out	255	L3	LVTTL	3.3	High	24	None	high	
address[7]	out	256	M3	LVTTL	3.3	High	24	None	high	
address[8]	out	259	N10	LVTTL	3.3	High	24	None	high	
address[9]	out	260	N9	LVTTL	3.3	High	24	None	high	
address[10]	out	261	K1	LVTTL	3.3	High	24	None	high	
address[11]	out	262	L1	LVTTL	3.3	High	24	None	high	
address[12]	out	269	M5	LVTTL	3.3	High	24	None	high	
address[13]	out	270	L6	LVTTL	3.3	High	24	None	high	
address[14]	out	271	L5	LVTTL	3.3	High	24	None	high	
address[15]	out	272	K2	LVTTL	3.3	High	24	None	high	
address[16]	out	275	L2	LVTTL	3.3	High	24	None	high	
address[17]	out	276	K4	LVTTL	3.3	High	24	None	high	
address[18]	out	277	L4	LVTTL	3.3	High	24	None	high	
address[19]	out	278	J3	LVTTL	3.3	High	24	None	high	
address[20]	out	281	J2	LVTTL	3.3	High	24	None	high	

Table 25. Pin assignment

Name	I/O	Pin CQ352	Pin CG624	Level	Volt.	Slew	Drive	Pull	Pol-arity	Note
address[21]	out	282	J1	LVTTL	3.3	High	24	None	high	
address[22]	out	283	L7	LVTTL	3.3	High	24	None	high	
address[23]	out	284	M7	LVTTL	3.3	High	24	None	high	Address, MSB
data[0]	inout	223	H2	LVTTL	3.3	High	24	None	high	Data, LSB
data[1]	inout	224	E2	LVTTL	3.3	High	24	None	high	
data[2]	inout	225	F2	LVTTL	3.3	High	24	None	high	
data[3]	inout	226	H4	LVTTL	3.3	High	24	None	high	
data[4]	inout	229	J4	LVTTL	3.3	High	24	None	high	
data[5]	inout	230	H5	LVTTL	3.3	High	24	None	high	
data[6]	inout	231	H6	LVTTL	3.3	High	24	None	high	
data[7]	inout	232	D2	LVTTL	3.3	High	24	None	high	
data[8]	inout	235	J6	LVTTL	3.3	High	24	None	high	
data[9]	inout	236	J5	LVTTL	3.3	High	24	None	high	
data[10]	inout	237	F3	LVTTL	3.3	High	24	None	high	
data[11]	inout	238	E3	LVTTL	3.3	High	24	None	high	
data[12]	inout	241	G4	LVTTL	3.3	High	24	None	high	
data[13]	inout	242	G3	LVTTL	3.3	High	24	None	high	
data[14]	inout	243	K8	LVTTL	3.3	High	24	None	high	
data[15]	inout	244	L8	LVTTL	3.3	High	24	None	high	Data, MSB
ramsn[0]	out	287	M2	LVTTL	3.3	High	24	None	low	SRAM chip select
ramsn[1]	out	288	P4	LVTTL	3.3	High	24	None	low	
ramsn[2]	out	-	P1	LVTTL	3.3	High	24	None	low	{reserved}
ramsn[3]	out	-	P6	LVTTL	3.3	High	24	None	low	{reserved}
ramsn[4]	out	-	P5	LVTTL	3.3	High	24	None	low	{reserved}
ramoen[0]	out	-	P3	LVTTL	3.3	High	24	None	low	{reserved}
ramoen[1]	out	-	N4	LVTTL	3.3	High	24	None	low	{reserved}
ramoen[2]	out	-	U1	LVTTL	3.3	High	24	None	low	{reserved}
ramoen[3]	out	-	T1	LVTTL	3.3	High	24	None	low	{reserved}
ramoen[4]	out	-	R2	LVTTL	3.3	High	24	None	low	{reserved}
rwen[0]	out	-	H3	LVTTL	3.3	High	24	None	low	{reserved}
rwen[1]	out	-	G2	LVTTL	3.3	High	24	None	low	{reserved}
rwen[2]	out	-	E1	LVTTL	3.3	High	24	None	low	{reserved}
rwen[3]	out	-	D1	LVTTL	3.3	High	24	None	low	{reserved}
ramben[0]	out	-	Y1	LVTTL	3.3	High	24	None	low	{reserved}
ramben[1]	out	-	P2	LVTTL	3.3	High	24	None	low	{reserved}
ramben[2]	out	-	K7	LVTTL	3.3	High	24	None	low	{reserved}
ramben[3]	out	-	K6	LVTTL	3.3	High	24	None	low	{reserved}
oen	out	296	N1	LVTTL	3.3	High	24	None	low	Output enable
writen	out	290	P7	LVTTL	3.3	High	24	None	low	Write strobe
read	out	295	R7	LVTTL	3.3	High	24	None	high	Read strobe

Table 25. Pin assignment

Name	I/O	Pin CQ352	Pin CG624	Level	Volt.	Slew	Drive	Pull	Pol-arity	Note
iosn	out	289	M1	LVTTL	3.3	High	24	None	low	IO area chip select
romsn[0]	out	-	N2	LVTTL	3.3	High	24	None	low	{reserved}
romsn[1]	out	-	R1	LVTTL	3.3	High	24	None	low	{reserved}
romsn[2]	out	-	AA3	LVTTL	3.3	High	24	None	low	{reserved}
romsn[3]	out	-	V3	LVTTL	3.3	High	24	None	low	{reserved}
brdyn	in	299	N3	LVTTL	3.3	-	-	Up	low	Bus ready
bexcn	in	305	P8	LVTTL	3.3	-	-	Up	low	Bus exception
pci_clk	in	300	G14	PCI	3.3					PCI clock
pci_rst	in	137	AB8	PCI	3.3					PCI reset
pci_frame	inout	180	AC9	PCI	3.3					
pci_irdy	inout	181	AA9	PCI	3.3					
pci_trdy	inout	182	AD6	PCI	3.3					
pci_stop	inout	184	AD5	PCI	3.3					
pci_idsel	in	161	U8	PCI	3.3					
pci_devsel	inout	183	AB9	PCI	3.3					
pci_par	inout	189	V10	PCI	3.3					
pci_perr	inout	187	V9	PCI	3.3					
pci_serr	inout	188	AD8	PCI	3.3					
pci_req	inout	143	EA11	PCI	3.3					
pci_gnt	in	142	EA10	PCI	3.3					
pci_int	out	136	W4	PCI	3.3					PCI interrupt
pci_cbe[0]	inout	205	W8	PCI	3.3					PCI byte enable, LSB
pci_cbe[1]	inout	190	W9	PCI	3.3					
pci_cbe[2]	inout	179	AE4	PCI	3.3					
pci_cbe[3]	inout	160	AE5	PCI	3.3					PCI byte enable, MSB
pci_ad[0]	inout	217	W11	PCI	3.3					PCI address/data, LSB
pci_ad[1]	inout	214	W12	PCI	3.3					
pci_ad[2]	inout	213	AA11	PCI	3.3					
pci_ad[3]	inout	212	Y11	PCI	3.3					
pci_ad[4]	inout	211	AE9	PCI	3.3					
pci_ad[5]	inout	208	AE6	PCI	3.3					
pci_ad[6]	inout	207	AE7	PCI	3.3					
pci_ad[7]	inout	206	Y10	PCI	3.3					
pci_ad[8]	inout	202	W10	PCI	3.3					
pci_ad[9]	inout	201	T13	PCI	3.3					
pci_ad[10]	inout	200	AB10	PCI	3.3					
pci_ad[11]	inout	199	AB11	PCI	3.3					
pci_ad[12]	inout	196	AD9	PCI	3.3					
pci_ad[13]	inout	195	AD10	PCI	3.3					
pci_ad[14]	inout	194	V11	PCI	3.3					

Table 25. Pin assignment

Name	I/O	Pin CQ352	Pin CG624	Level	Volt.	Slew	Drive	Pull	Pol-arity	Note
pci_ad[15]	inout	193	AD7	PCI	3.3					
pci_ad[16]	inout	173	AC8	PCI	3.3					
pci_ad[17]	inout	172	AB7	PCI	3.3					
pci_ad[18]	inout	171	AC7	PCI	3.3					
pci_ad[19]	inout	170	AA8	PCI	3.3					
pci_ad[20]	inout	167	Y8	PCI	3.3					
pci_ad[21]	inout	166	V8	PCI	3.3					
pci_ad[22]	inout	165	V7	PCI	3.3					
pci_ad[23]	inout	164	Y7	PCI	3.3					
pci_ad[24]	inout	159	W7	PCI	3.3					
pci_ad[25]	inout	158	AC5	PCI	3.3					
pci_ad[26]	inout	155	AC6	PCI	3.3					
pci_ad[27]	inout	154	Y6	PCI	3.3					
pci_ad[28]	inout	153	W6	PCI	3.3					
pci_ad[29]	inout	152	AB6	PCI	3.3					
pci_ad[30]	inout	147	AA6	PCI	3.3					
pci_ad[31]	inout	146	Y3	PCI	3.3					PCI address/data, MSB
txd[1]	out	342	L19	LVTTL	3.3	Low	12	None	low	UART data transmit
rxd[1]	in	343	J23	LVTTL	3.3	-	-	None	low	UART data receive
rtsn[1]	out	338	J20	LVTTL	3.3	Low	12	None	low	Ready to Send
ctsn[1]	in	341	J21	LVTTL	3.3	-	-	None	low	Clear to Send
txd[2]	out	336	K20	LVTTL	3.3	Low	12	None	low	UART data transmit
rxd[2]	in	337	D25	LVTTL	3.3	-	-	None	low	UART data receive
rtsn[2]	out	332	E25	LVTTL	3.3	Low	12	None	low	Ready to Send
ctsn[2]	in	335	K19	LVTTL	3.3	-	-	None	low	Clear to Send
wdogn	out	319	D20	LVTTL	3.3	Low	12	None	low	Watchdog timeout
gpio[0]	inout	113	F24	LVTTL	3.3	Low	12	None	high	General purpose I/O
gpio[1]	inout	112	G24	LVTTL	3.3	Low	12	None	high	{interrupt # 1}
gpio[2]	inout	111	K18	LVTTL	3.3	Low	12	None	high	{interrupt # 2}
gpio[3]	inout	110	L18	LVTTL	3.3	Low	12	None	high	{interrupt # 3}
gpio[4]	inout	107	H22	LVTTL	3.3	Low	12	None	high	{interrupt # 4}
gpio[5]	inout	106	J22	LVTTL	3.3	Low	12	None	high	{interrupt # 5}
gpio[6]	inout	105	G22	LVTTL	3.3	Low	12	None	high	{interrupt # 6}
gpio[7]	inout	104	M17	LVTTL	3.3	Low	12	None	high	{interrupt # 7}
gpio[8]	inout	101	H20	LVTTL	3.3	Low	12	None	high	{interrupt # 8}
gpio[9]	inout	100	H19	LVTTL	3.3	Low	12	None	high	{interrupt # 9}
gpio[10]	inout	99	E18	LVTTL	3.3	Low	12	None	high	{interrupt # 10}
gpio[11]	inout	98	F18	LVTTL	3.3	Low	12	None	high	{interrupt # 11}
gpio[12]	inout	95	G21	LVTTL	3.3	Low	12	None	high	{interrupt # 12}
gpio[13]	inout	94	G20	LVTTL	3.3	Low	12	None	high	{interrupt # 13}

Table 25. Pin assignment

Name	I/O	Pin CQ352	Pin CG624	Level	Volt.	Slew	Drive	Pull	Pol-arity	Note
gpio[14]	inout	93	F20	LVTTL	3.3	Low	12	None	high	{interrupt # 14}
gpio[15]	inout	92	F19	LVTTL	3.3	Low	12	None	high	{non-maskable interrupt # 15}
gpio[16]	inout	86	N19	LVTTL	3.3	Low	12	None	high	
gpio[17]	inout	85	M21	LVTTL	3.3	Low	12	None	high	
gpio[18]	inout	84	M20	LVTTL	3.3	Low	12	None	high	
gpio[19]	inout	83	N17	LVTTL	3.3	Low	12	None	high	
gpio[20]	inout	82	K24	LVTTL	3.3	Low	12	None	high	
gpio[21]	inout	79	L24	LVTTL	3.3	Low	12	None	high	
gpio[22]	inout	78	L20	LVTTL	3.3	Low	12	None	high	
gpio[23]	inout	77	L21	LVTTL	3.3	Low	12	None	high	
gpio[24]	inout	76	F25	LVTTL	3.3	Low	12	None	high	
gpio[25]	inout	73	G25	LVTTL	3.3	Low	12	None	high	
gpio[26]	inout	72	K22	LVTTL	3.3	Low	12	None	high	
gpio[27]	inout	71	L22	LVTTL	3.3	Low	12	None	high	
gpio[28]	inout	70	M18	LVTTL	3.3	Low	12	None	high	
gpio[29]	inout	67	M19	LVTTL	3.3	Low	12	None	high	
gpio[30]	inout	66	H23	LVTTL	3.3	Low	12	None	high	
gpio[31]	inout	65	E24	LVTTL	3.3	Low	12	None	high	

Table 25. Pin assignment

Name	I/O	Pin CQ352	Pin CG624	Level	Volt.	Slew	Drive	Pull	Pol-arity	Note
spw_clk	in	314	G14	LVTTL	3.3	-	-	-	-	SpaceWire clock
spw_rxd[0]	in	43	P19	LVDS	2.5	-	-	-	high	SpaceWire data
spw_rxdn[0]	in	42	P20	LVDS	2.5	-	-	-	low	
spw_rxs[0]	in	41	P23	LVDS	2.5	-	-	-	high	SpaceWire strobe
spw_rxsn[0]	in	40	R23	LVDS	2.5	-	-	-	low	
spw_txd[0]	out	37	P25	LVDS	2.5	-	-	-	high	SpaceWire data
spw_txdn[0]	out	36	R25	LVDS	2.5	-	-	-	low	
spw_txs[0]	out	35	P22	LVDS	2.5	-	-	-	high	SpaceWire strobe
spw_txsn[0]	out	34	R22	LVDS	2.5	-	-	-	low	
spw_rxd[1]	in	31	R18	LVDS	2.5	-	-	-	high	SpaceWire data
spw_rxdn[1]	in	30	T18	LVDS	2.5	-	-	-	low	
spw_rxs[1]	in	29	R24	LVDS	2.5	-	-	-	high	SpaceWire strobe
spw_rxsn[1]	in	28	T24	LVDS	2.5	-	-	-	low	
spw_txd[1]	out	25	T25	LVDS	2.5	-	-	-	high	SpaceWire data
spw_txdn[1]	out	24	U25	LVDS	2.5	-	-	-	low	
spw_txs[1]	out	23	R20	LVDS	2.5	-	-	-	high	SpaceWire strobe
spw_txsn[1]	out	22	T20	LVDS	2.5	-	-	-	low	
spw_rxd[2]	in	19	T19	LVDS	2.5	-	-	-	high	SpaceWire data
spw_rxdn[2]	in	18	U19	LVDS	2.5	-	-	-	low	
spw_rxs[2]	in	17	W25	LVDS	2.5	-	-	-	high	SpaceWire strobe
spw_rxsn[2]	in	16	Y25	LVDS	2.5	-	-	-	low	
spw_txd[2]	out	13	AA25	LVDS	2.5	-	-	-	high	SpaceWire data
spw_txdn[2]	out	12	AB25	LVDS	2.5	-	-	-	low	
spw_txs[2]	out	11	U20	LVDS	2.5	-	-	-	high	SpaceWire strobe
spw_txsn[2]	out	10	V20	LVDS	2.5	-	-	-	low	
cantx[0]	out	326	M25	LVTTL	3.3	Low	12	None	low	CAN 0 tx data
canrx[0]	in	325	N25	LVTTL	3.3	-	-	None	low	CAN 0 rx data
canen[0]	out	-	H24	LVTTL	3.3	Low	12	None	-	{reserved}
cantx[1]	out	324	L23	LVTTL	3.3	Low	12	None	low	CAN 1 tx data
canrx[1]	in	323	N16	LVTTL	3.3	-	-	None	low	CAN 1 rx data
canen[1]	out	-	J24	LVTTL	3.3	Low	12	None	-	{reserved}

Table 25. Pin assignment

Name	I/O	Pin CQ352	Pin CG624	Level	Volt.	Slew	Drive	Pull	Pol-arity	Note
busainen	out	58	N23	LVTTL	3.3	Low	12	None	high	Mil-Std-1553
busainn	in	54	N22	LVTTL	3.3	-	-	None	low	bus 0
busainp	in	55	M22	LVTTL	3.3	-	-	None	high	nominal
busaoutin	out	61	P17	LVTTL	3.3	Low	12	None	high	
busaoutn	out	59	M23	LVTTL	3.3	Low	12	None	low	
busaoutp	out	60	P18	LVTTL	3.3	Low	12	None	high	
busbinen	out	48	N24	LVTTL	3.3	Low	12	None	high	Mil-Std-1553
busbinn	in	46	N18	LVTTL	3.3	-	-	None	low	bus 0
busbinp	in	47	J25	LVTTL	3.3	-	-	None	high	redundant
busboutin	out	53	K25	LVTTL	3.3	Low	12	None	high	
busboutn	out	49	M24	LVTTL	3.3	Low	12	None	low	
busboutp	out	52	L25	LVTTL	3.3	Low	12	None	high	

Pins not used should be left unconnected (or tied to ground), including the pins marked as *{reserved}*. The only exception is if the unused pin is mapped on a hardwired clock input or a routed clock input, which should then be tied to ground:

CQ352 package: 122, 123, 128, 129, 136, 137, 142, 143, 299, 300, 305, 306, 313, 314, 319, 320

CG624 package: AC12, AC13, AD12, AD13, W14, W15, W13, Y13, B13, B14, C12, C13, G12, G13, G14, G15

For the usage of all other pins, please refer to the specific pins of the selected package, as described in the next sections and the Actel data sheet [RTAX].

17.3 RTAX2000S specific pins - CQ352 package

The Actel RTAX2000S FPGA device has special pins that need to be correctly connected on the printed circuit board, as shown in table 26. Please refer to the Actel data sheet [RTAX] for details.

Table 26. RTAX2000S special pins - CQ352 package

Name	Pin CQ352	Note
GND	1, 9, 15, 21, 27, 33, 39, 45, 51, 57, 63, 69, 75, 81, 88, 89, 97, 103, 109, 115, 121, 133, 145, 151, 157, 163, 169, 176, 177, 186, 192, 198, 204, 210, 216, 222, 228, 234, 240, 246, 252, 258, 264, 265, 274, 280, 286, 292, 298, 310, 322, 330, 334, 340, 345, 352	Low supply voltage, ground
VCCA	3, 14, 32, 56, 74, 87, 102, 114, 150, 162, 175, 191, 209, 233, 251, 263, 279, 291, 329, 339	1.5 V supply voltage for array
VCCDA	2, 44, 90, 91, 116, 117, 130, 131, 132, 148, 149, 174, 178, 221, 266, 268, 293, 294, 307, 308, 309, 327, 328, 346	3.3 V supply voltage for I/O differential amplifier and JTAG and probe interfaces.
VCCIB0	321, 333, 344	3.3 V supply voltage for I/O
VCCIB1	273, 285, 297	3.3 V supply voltage for I/O
VCCIB2	227, 239, 245, 257	3.3 V supply voltage for I/O
VCCIB3	185, 197, 203, 215	3.3 V supply voltage for I/O
VCCIB4	144, 156, 168	3.3 V supply voltage for I/O
VCCIB5	96, 108, 120	3.3 V supply voltage for I/O
VCCIB6	50, 62, 68, 80	3.3 V supply voltage for I/O
VCCIB7	8, 20, 26, 38	2.5 V supply voltage for I/O
VPUMP	267	Voltage External Pump. In normal operation, using the internal charge pump, should be tied to ground.
TRST	351	JTAG Test Clock. Actel recommends this pin be hardwired to ground for flight.
TCK	349	JTAG Test Clock. Actel recommends this pin be hardwired to ground. Must not be left unconnected.
TDI	348	JTAG Test Data Input. Actel recommends this pin be hardwired to VCCDA, or left unconnected.
TDO	347	JTAG Test Data Output. Must be left unconnected.
TMS	350	JTAG Test Mode Select. Actel recommends that this pin be hardwired to VCCDA, or left unconnected.
PRA	312	Test Probe. The pins' probe capabilities are disabled to protect programmed design confidentiality. These pins must be left unconnected.
PRB	311	
PRC	135	
PRD	134	
NC	124, 125, 126, 127, 138, 139, 140, 141, 301, 302, 303, 304, 315, 316, 317, 318	No Connection. Pins are not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
CLK*	122, 123, 128, 129, 136, 137, 142, 143	Global clocks. When pins are unused, Actel recommends they are tied to known state, preferably ground.
HCLK*	299, 300, 305, 306, 313, 314, 319, 320	Hardwired clocks. When pins are unused, it is recommended that they are tied to ground.

17.4 RTAX2000S specific pins - CG624 package

The Actel RTAX2000S FPGA device has special pins that need to be correctly connected on the printed circuit board, as shown in table 26. Please refer to the Actel data sheet [RTAX] for details.

Table 27. RTAX2000S special pins - CG624 package

Name	Pin CG624	Note
GND	A18, A24, A25, A2, A8, AA10, AA16, AA18, AA21, AA5, AB22, AB4, AC10, AC16, AC23, AC3, AD1, AD2, AD24, AD25, AE1, AE18, AE24, AE2, AE25, AE8, B1, B2, B25, B24, C10, C16, C23, C3, D22, D4, E10, E16, E21, E5, E8, H1, H21, H25, K21, K23, K3, K5, L11, L12, L13, L14, L15, M11, M12, M13, M14, M15, N11, N12, N13, N14, N15, P11, P12, P13, P14, P15, R11, R12, R13, R14, R15, T21, T23, T3, T5, V1, V25, V5	Low supply voltage, ground
VCCA	AB20, F22, F4, J17, J9, K10, K11, K15, K16, L10, L16, R10, R16, T10, T11, T15, T16, U17, U9, Y4	1.5 V supply voltage for array
VCCDA	A12, A14, AA13, AA15, AA20, AA7, AB13, AC11, AD11, AD4, AE12, AE17, B15, C15, C6, D13, E13, E19, F21, G10, G5, N21, N5, W21	3.3 V supply voltage for I/O differential amplifier and JTAG and probe interfaces.
VCCIB0	A3, B3, C4, D5, E13, J10, J11, K12	3.3 V supply voltage for I/O
VCCIB1	A23, B23, C22, D21, J15, J16, K14	3.3 V supply voltage for I/O
VCCIB2	C24, C25, D23, E22, K17, L17, M16	3.3 V supply voltage for I/O
VCCIB3	AA22, AB23, AC24, AC25, P16, R17, T17	2.5 V supply voltage for I/O
VCCIB4	AB21, AC22, AD23, AE23, T14, U15, U16	3.3 V supply voltage for I/O
VCCIB5	AB5, AC4, AD3, AE3, T12, U10, U11	3.3 V supply voltage for I/O
VCCIB6	AA4, AB3, AC1, AC2, P10, R9,T9	3.3 V supply voltage for I/O
VCCIB7	C1, C2, D3, E4, K9, L9, M10	3.3 V supply voltage for I/O
VPUMP	E20	Voltage External Pump. In normal operation, using the internal charge pump, should be tied to ground.
TRST	E6	JTAG Test Clock. Actel recommends this pin be hardwired to ground for flight.
TCK	F5	JTAG Test Clock. Actel recommends this pin be hardwired to ground. Must not be left unconnected.
TDI	C5	JTAG Test Data Input. Actel recommends that this pin be hardwired to VCCDA, or left unconnected.
TDO	F6	JTAG Test Data Output. Must be left unconnected.
TMS	D6	JTAG Test Mode Select. Actel recommends this pin be hardwired to VCCDA, or left unconnected.
PRA	F13	Test Probe. The pins' probe capabilities are disabled to protect programmed design confidentiality. These pins must be left unconnected.
PRB	A13	
PRC	AB12	
PRD	AE13	
NC	AA12, AA14, E12, E14, F12, F14, H12, H14, J12, J14, U12, U14, V12, V14, Y12, Y14	No Connection. Pins are not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
CLK*	AC12, AC13, AD12, AD13, W14, W15, W13, Y13	Global clocks. When pins are unused, Actel recommends they are tied to known state, preferably ground.
CLKH*	B13, B14, C12, C13, G12, G13, G14, G15	Hardwired clocks. When pins are unused, it is recommended that they are tied to ground.

18 Reference documents

[AMBA] AMBA™ Specification, Rev 2.0, ARM IHI 0011A, 13 May 1999, Issue A, first release, ARM Limited

[GRLIB] GRLIB IP Library User's Manual, Version 1.0.15, Gaisler Research, www.gaisler.com

[GRIP] GRLIB IP Core User's Manual, Version 1.0.15, Gaisler Research, www.gaisler.com

[SPW] ECSS - Space Engineering, SpaceWire - Links, Nodes, Routers and Networks, ECSS-E-50-12A, 24 January 2003

[RMAPID] Space Engineering, Protocol Identification, Draft ECSS-E50-11, Draft B February 2005

[RMAP] Space Engineering, Remote Memory Access Protocol, Draft ECSS-E50-11, Draft F December 2006 *1*

[RTAX] RTAX-S RadTolerant FPGAs, 5172169-8/5.07, v4.0, May 2007, Actel Corporation

[PACK] Package Mechanical Drawings, 5193068-19/5.07, v9.5, May 2007, Actel Corporation

Note 1: The ECSS-E50-11 Draft F document of the draft standard contains an informative VHDL description of the CRC implementation used in the RMAP protocol which is considered as incorrect with respect to the normative part of the draft standard. The VHDL descriptions in the ECSS-E50-11 Draft F document should therefore be ignored.

19 Ordering information

Ordering information is provided in table 28 and a legend is provided in table 29.

Table 28. Ordering information

Product	Device	Speed Grade		Package Type	Package Lead Count	Application	
		Std	-1			E	B
GR701A	RTAX2000S		-1	CQ	352	E	B

Table 29. Ordering legend

Designator	Option	Description
Product	GR701A	PCI to SpaceWire and 1553 bridge
Device	RTAX2000S	2,000,000 Equivalent System Gates
Speed Grade	STD	Standard Speed
	-1	Approximately 15% Faster than Standard
Package Type	CQ	Ceramic Quad Flat Pack
	CG	Ceramic Column Grid Array
	LG	Land Grid Array
	FG	Fine Pitch Plastic Ball Grid Array
Application	B	MIL-STD 883 Class B
	E	E-Flow (Actel Space-Level Flow)

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