

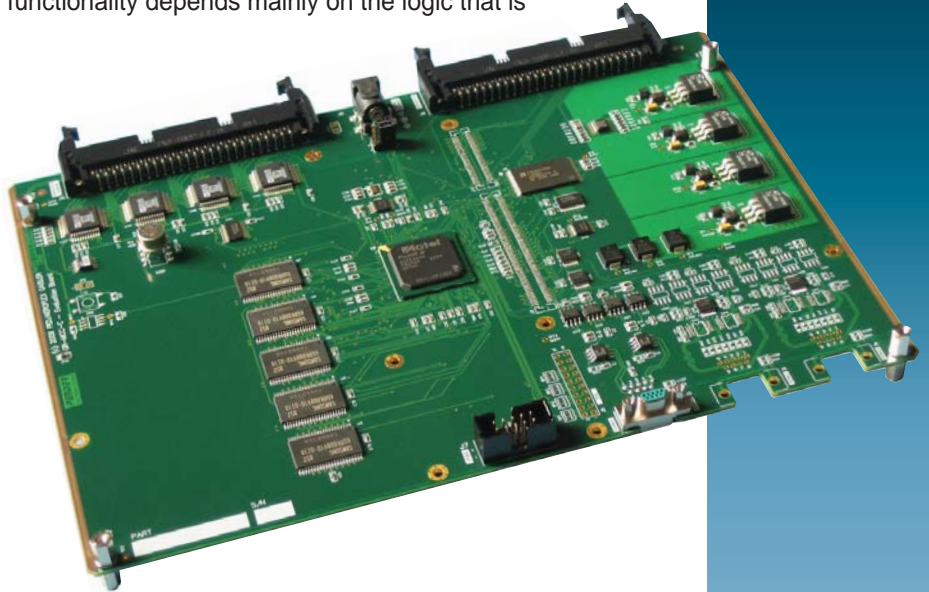
# LEON ProASIC3/RT ProASIC3 Development Board GR-MCC-C



## Description

The GR-MCC-C FPGA board has been created to support early development and fast prototyping of digital and analogue computer designs. The board incorporates a footprint for an Actel ProASIC3E, ProASIC3L or RT ProASIC3 field programmable gate array (FPGA) device and is capable of operating stand-alone or in conjunction with other boards. To provide more I/O possibilities, additional mezzanine and accessory boards are available. As the board is based on a re-programmable FPGA device, the actual functionality depends mainly on the logic that is designed and incorporated in the FPGA.

Whilst the board is perfectly suitable as a general purpose development platform for any ProASIC3E/L or RT ProASIC3 project, the incorporation of on-board volatile (SRAM) and non-volatile memories (Flash PROM), together with four octal 12-bit ADC devices, LVDS, CAN and JTAG interfaces makes the board ideal for implementing LEON based designs. Additionally, the design of this board can support the implementation of LEON-FT fault-tolerant systems.



## Features

- Actel ProASIC3E or ProASIC3L FPGA in 484-pin Fine Pitch Ball Grid Array package, or RT ProASIC3 FPGA in 484-pin Ceramic Column Grid Array package, or a socket
- Double-Euro style PCB
- On-board memory:
  - SRAM
  - FLASH PROM
- Dual LVDS transceivers
- Dual CAN transceivers
- Four octal 12-bit ADC devices providing 32 analogue input channels (of which 5 are used internally)
- PIO expansion options: RS232, RS422, LVDS, CAN, TM & TC, PacketWire
- User I/O mezzanine expansion options: Mil-Std-1553B, Ethernet, TM & TC, I<sup>2</sup>C
- JTAG interface for programming and debug link
- On-board oscillator
- On-board power regulators
- Suitable for Single Event Upset (SEU) testing
- Form Fit and Functional Equivalent (FFFE) flight components available
- LEON3/LEON4 and LEON3FT compatible FPGA template designs available

### CONTACT INFORMATION

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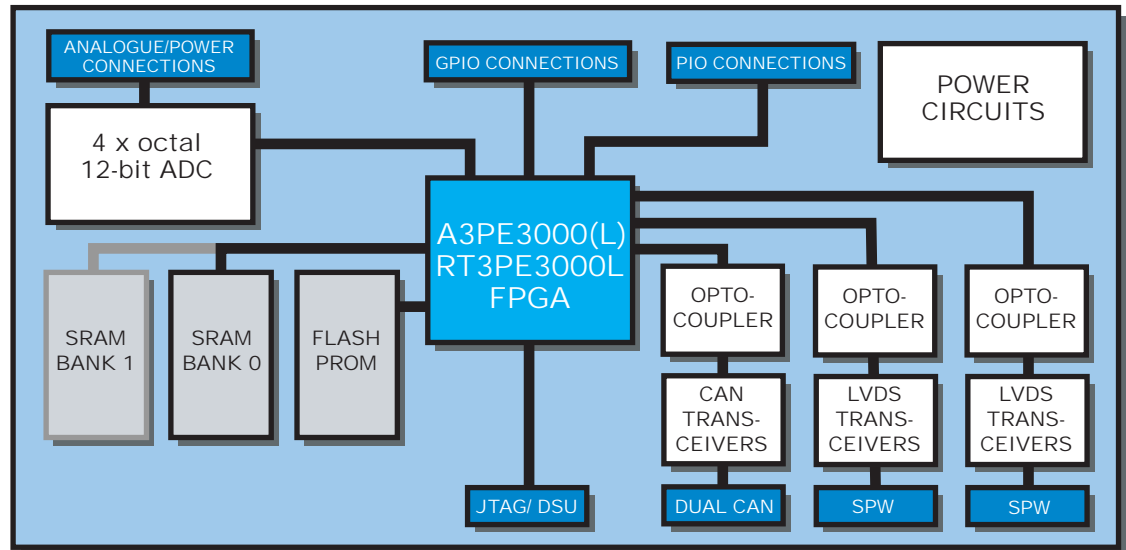
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## LEON3/LEON4 applications and support

The LEON processors are synthesizable VHDL models of 32-bit processors compliant to the SPARC V8 architecture developed by Aeroflex Gaisler. The LEON designs are unique in their source-code availability, offering the user extensive configuration options and full flexibility in the use and extension of the cores' functions to suit the user's specific application and interfaces.

The standard LEON implementation is targeted for commercial designs while the Fault Tolerant (FT) version is targeted for use in Aerospace and Critical applications with fault tolerance features including internal upset resistant structures, register parity protection and EDAC for external memories.

For more information on the LEON3 and LEON4 cores, the VHDL models, synthesis, configuration, hardware and software development tools, IP core developments and Real-Time Operating Systems, please refer to the Aeroflex Gaisler web-site ([www.aeroflex.com/gaisler](http://www.aeroflex.com/gaisler)).



## Specifications

- Double-Euro style PCB (233.5mm x 160mm) form factor
- Actel ProASIC3E or ProASIC3L FPGA in 484-pin FBGA package (A3PE3000(L)-FGG484), or RT ProASIC3 FPGA in 484-pin CCGA package (RT3PE3000L-CG484B), or optional socket (Actel SE-FGG484-S-H)
- Typical core speeds 20 to 30 MHz (depending on speed grade and core configuration)
- One bank of 8 Mbyte (2M x 32+8 bit) 3.3V SRAM memory on-board (2nd bank optional)
- One bank of 8 Mbyte (8M x 8 bit) 5V Flash PROM memory on-board (with 5V to 3.3V level shifter)
- Dual LVDS transceivers (with opto-isolation) for two SpaceWire interfaces (10 MBPS limitation)
- Dual CAN transceivers (ISO11898, with opto-isolation)
- Four octal 12-bit ADC devices (AD7891) providing 32 analogue inputs (with 5V to 3.3V level shifter)
- 16 PIO expansion (2x10 pin 0.1" header) compatible with accessory boards
- I/O expansion with 60 and 120 pin connectors (AMP 177-984-2/5) compatible with mezzanine boards
- On-board 25 MHz oscillator, power on reset, reset button
- On-board linear regulators supply 5V, 3.3V and 1.5V generated from single +7V input

The interface connectors on the front edge of the board provide:

- Dual CAN interface (MDM9P connector)
- Two SpaceWire interfaces (MDM9S connectors)
- JTAG – Debug Support Unit (DSU) interface (2x5 pin 0.1" header)

The interface connectors on the back edge of the board provide:

- 60 GPIO pins (two 2x25 pin 0.1" headers)
- Analogue connections (two 2x25 pin 0.1" headers)
- 2.1mm connector for external +7V DC power supply