

Aeroflex Gaisler's LEON3 SPARC processor on Synopsys HAPS development platform



Introduction

Aeroflex Gaisler provides system-on-a-chip (SoC) solutions for exceptionally competitive markets such as aerospace, military and demanding commercial applications. Aeroflex Gaisler's products consist of user-customizable 32-bit SPARC V8 processor cores, peripheral IP-cores and associated software and development tools. The key product is the LEON3 32-bit SPARC processor core (LEON3).

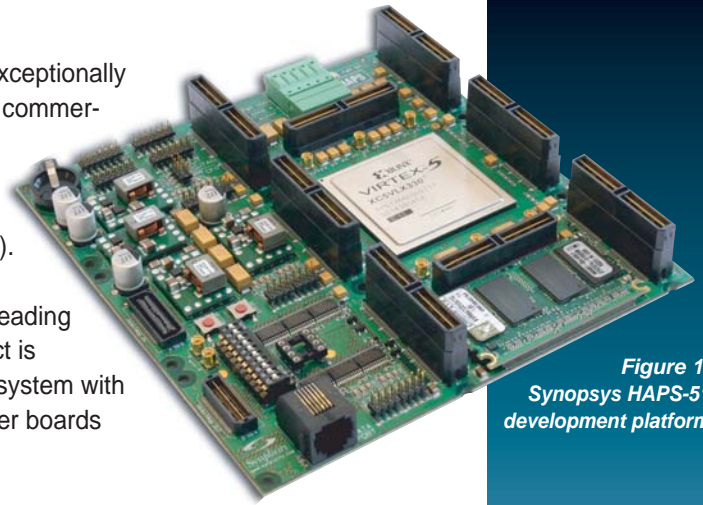


Figure 1: Synopsys HAPS-51 development platform

Synopsys Hardware Platforms Group (www.synopsys.com) is a leading provider of off-the-shelf ASIC prototyping boards. The key product is HAPS (High-performance ASIC Prototyping System), a modular system with multi-FPGA motherboards and standard or custom-made daughter boards which can be stacked together in a variety of ways.

Aeroflex Gaisler's GRLIB IP library environment includes support for HAPS development platforms, providing example designs and board support packages used with Synopsys synthesis tools and Xilinx place & route tools.

Hardware development

A HAPS specific example design is depicted in the block diagram. It features a LEON3 32-bit SPARC processor with a debug support unit, memory controllers, on-chip memory, general purpose input output, timers, etc. When downloaded onto the FPGA of a HAPS motherboard, the design enables control of on-board resources such as processor, memories and I/O ports. Access to a variety of daughter boards, such as BIO1, DDR_1x1, SRAM_1x1, SDRAM_1x1, FLASH_1x1 and GEPHY_1x1 is supported by including HAPS tailored IP cores.

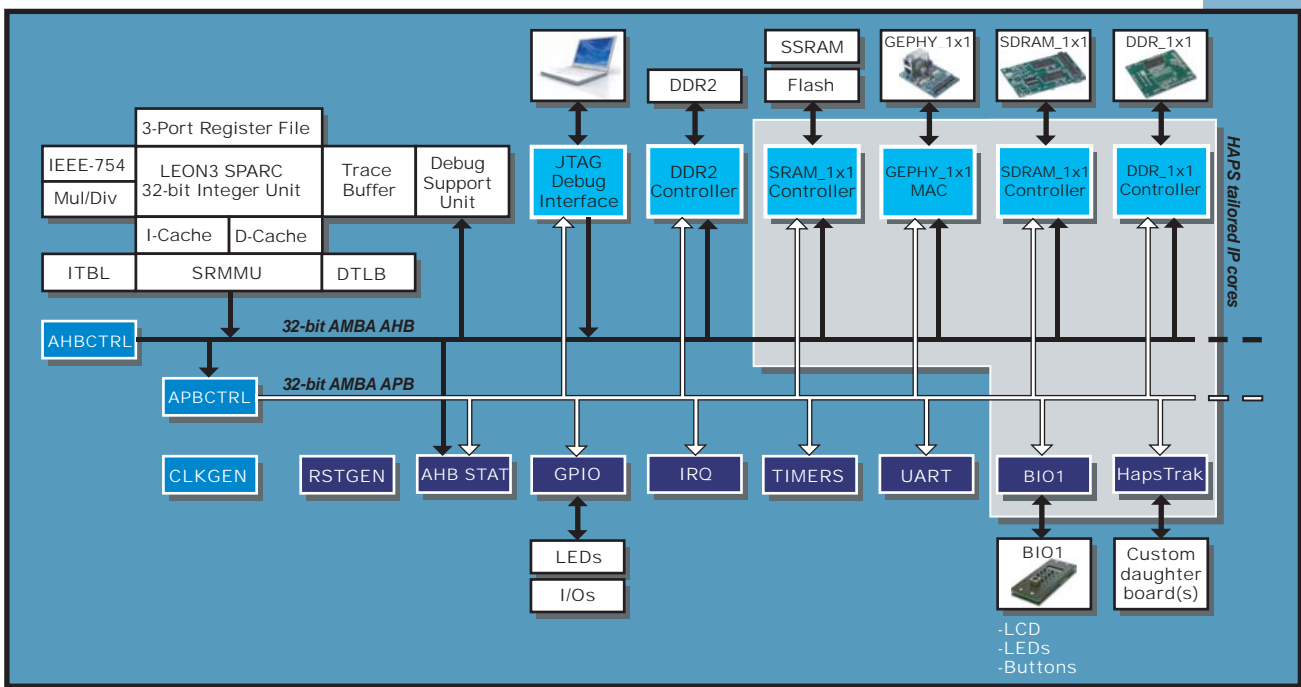


Figure 2: Aeroflex Gaisler's LEON3 based system-on-a-chip design for HAPS-51 using the GRLIB IP library

Software development

Software for the LEON3 system may be written in ANSI-C and compiled using the BCC cross compiler. Development and debugging of software is facilitated by Aeroflex Gaisler's GRMON debug monitor. The monitor communicates with the LEON3 debug support unit and provides complete access to all memory and registers of the system. Upload and execution of software is supported, as well as single-stepping, disassembly, monitoring of on-chip bus traffic etc. Communication to and from the host system (Linux or Windows PC) is provided through a standard JTAG interface.

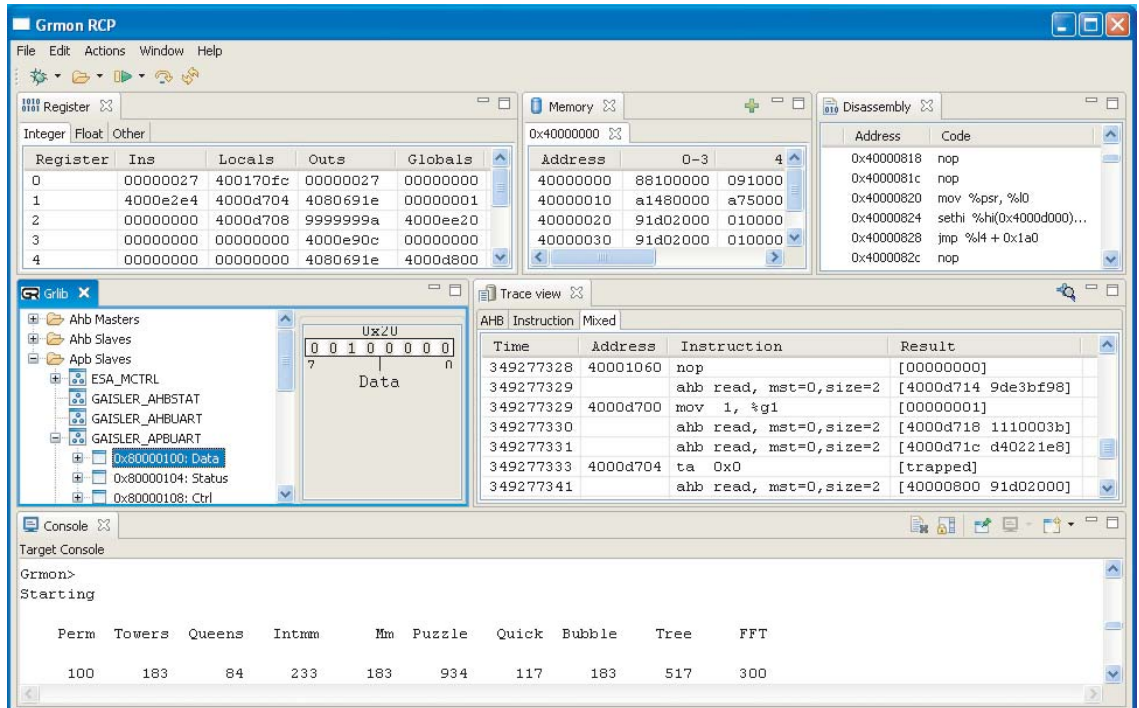


Figure 3: Gaisler Research's GRMON monitor program

HAPS development suite

Aeroflex Gaisler's HAPS development suite comprises everything needed in order to develop a LEON3 based system-on-a-chip design for a HAPS platform.

The suite includes:

- GRLIB VHDL IP library, containing LEON3 source code etc.
- Template designs (HAPS-31, HAPS-51, HAPS-52, HAPS-54 etc.)
- Bare-C Cross-compiler system (BCC)
- GRMON debug monitor software



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For more information about HAPS, visit www.synopsys.com

For more information and downloads, visit www.aeroflex.com/gaisler and proceed to Products ► IP Cores ► HAPS

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