

# LEON3

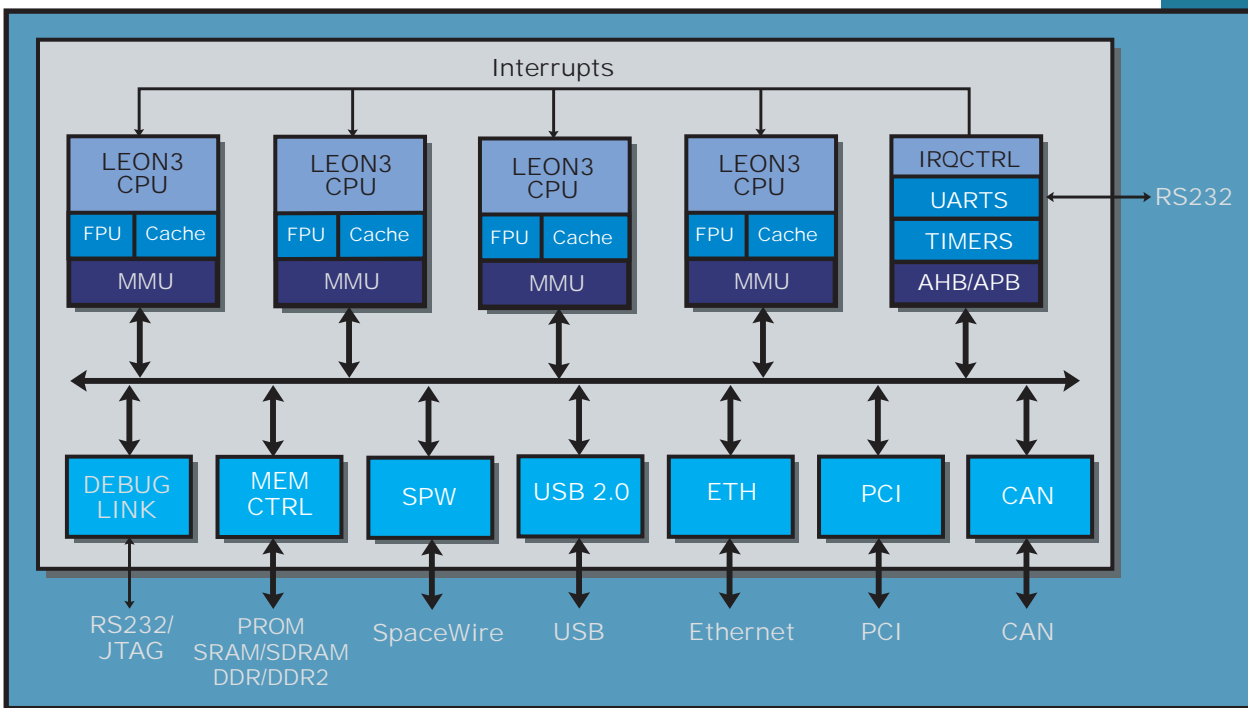
## Multiprocessing CPU Core



### General

The LEON3 is a 32-bit processor based on the SPARC V8 architecture with support for multiprocessing configurations. The processor is fully synthesizable and up to 16 CPU cores can be implemented in asymmetric multiprocessing (AMP) or synchronous multiprocessing (SMP) configurations. A typical configuration with four processors is capable of delivering up to 1600 Dhrystone MIPS of performance. The LEON3 multiprocessor core is available in full source code under the GNU GPL license for evaluation, research and educational purposes. A low cost license is available for commercial applications.

The LEON3 multiprocessor solution gives higher performance at lower frequencies than single processor solutions. This brings significant cost and power savings, while maintaining full compatibility with existing EDA tools and development flows. The LEON3 processor simplifies complex multiprocessor system design, therefore reducing time-to-market and design costs.



### Architecture

LEON3 can be utilized in both SMP and AMP configurations. The processor provides hardware support for cache coherency, processor enumeration and interrupts steering. A unique debug interface allows non-intrusive hardware debugging of both single- and multiple-processor systems, and provides access to all on-chip registers and memory. Trace buffers for both instructions and AMBA bus traffic are also available. An AMBA round-robin arbiter provides fair bus utilization for the processors.

Each core can be configured to use an IEEE-754 compliant FPU for floating-point operations (for area critical designs one FPU can be shared between CPU cores).

A SPARC Reference Memory Management Unit (MMU) is provided for advanced memory management and protection.

## Flexibility

The LEON3 multiprocessor solution is highly configurable. The configuration of each processor in terms of cache size, FPU and MMU usage can be individually defined. Asymmetric configurations, such as two main processors with FPU and MMU and two I/O processors are supported. The LEON3 multiprocessor system takes full advantage of the plug&play capabilities of the GRLIB IP-library, increasing flexibility and reducing development time.

## Software

For SMP configurations, the operating systems Linux 2.6 SMP and eCos have been ported for LEON3. The Linux 2.6 SMP is able to automatically load balance applications across multiple LEON3 cores, providing the most advanced hardware/software architecture for high performance systems. For loosely coupled (message passing) AMP configurations, operating systems such as RTEMS and  $\mu$ CLinux are available.

## Features

### ■ Highly configurable

Flexible implementation using between 1 and 16 processors.  
Sizing of both data and instruction cache between 0k and 2Mbytes across each CPU.  
IP library with plug&play functionality allowing rapid and flexibility during SoC design.  
Optional high performance IEEE-754 Floating Point Unit.  
Optional SPARC Reference Memory Management Unit.

### ■ High performance

SPARC V8 architecture multiprocessor-capable instruction set architecture.  
400 MHz on a 0.13  $\mu$ m process, giving up to 6400 Dhrystone MIPS of performance.  
Built-in cache snooping for data coherency.

### ■ Energy efficient

Power down mode:  
Individual processor shutdown providing significant energy saving on dynamic power consumption.  
Clock gating:  
Each processor's clock CPU can be individually gated-off in power down mode for further reduction of both dynamic and static power consumption.

### ■ Simple design integration

Supported by the plug&play capabilities of the GRLIB IP-library, increasing flexibility and reducing development time.

### ■ Software support environment

eCos or Linux 2.6 SMP operating system for SMP configurations.  
RTEMS, VxWorks,  $\mu$ CLinux or ThreadX operating system for AMP configurations.

### ■ Availability

Source VHDL code or Netlist.

## CONTACT INFORMATION

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