# GR712RC
## Dual Core LEON3-FT

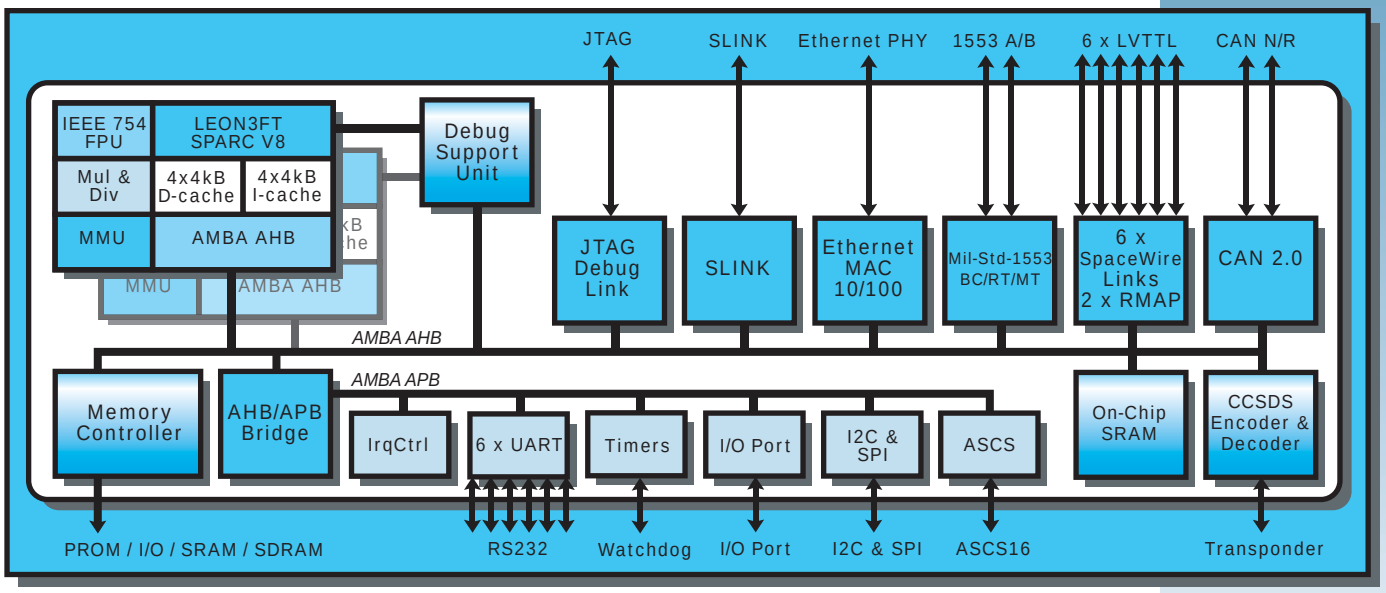
AEROFLEX GAISLER

### Introduction
The GR712RC is a dual core LEON3-FT SPARC V8 processor, with advanced interface protocols, dedicated for high reliability rad-hard aerospace applications.

The GR712RC is fabricated at Tower Semiconductors Ltd., using standard 0.18µm CMOS technology. It employs Rad-Hard-By-Design methods from Aeroflex Gaisler and Ramon Chips, enabling superior radiation hardness.

The GR712RC can be utilized in symmetric or asymmetric multiprocessing mode. The processors provide hardware support for cache coherency, processor enumeration and interrupt steering. Each processor core includes a SPARC Reference Memory Management Unit (SRMMU) and an IEEE-754 compliant FPU for floating-point operations. At maximum frequency the GR712RC delivers up to 200 DMIPS and 200 MFLOPS.


### Software
For SMP configurations, the operating systems VxWorks 6.7, Linux 2.6 SMP and eCos have been ported for the GR712RC. Linux 2.6 SMP and VxWorks 6.7 are able to automatically load balance applications across the processor cores, providing the most advanced hardware/software architecture for high performance systems. For loosely coupled (message passing) AMP configurations, operating systems such as RTEMS and µCLinux are available.




### Availability
The GR712RC is available as engineering samples. Space qualified parts will be available in Q2 2013. Prototyping and evaluation is possible using the GR712RC development board.

SPARC Compliant SCD V8

## Main Features

- Technology: 0.18 µm standard CMOS, Tower Semiconductors Ltd.
- Library: 0.18 µm RadSafe™, Ramon Chips Ltd.
- Package and operating range:
  - 240 pin CQFP, 0.5 mm pitch, 32 mm x 32 mm, hermetically sealed, delivered with flat pins and insulating lead-frame for customer trim and form
  - Core voltage 1.8V +/– 0.15V, I/O voltage 3.3V +/– 0.3V
  - Temperature range –55°C to +125°C
- Radiation tolerance:
  - TID: 300 krad(Si), SEL: Immune > 118 MeV-cm²/mg at +125°C, proven SEU tolerance with hardened flip-flops and error correction of all on-chip memories
- Screening and qualification:
  - Equivalent to MIL-STD-883 Class level S
- Maximum clock frequency 100 MHz (depending on external memory device selection)
  - Optional 2x internal frequency multiplication by an all-digital DLL
  - Optional 2x or 4x internal SpaceWire frequency multiplication by an all-digital DLL
  - Clock-gating for each major core
- Two LEON3-FT SPARC V8 compliant 32-bit processors, each with:
  - 16 KiB multi-way instruction cache and 16 KiB multi-way data cache
  - SPARC reference memory management unit (SRMMU) with 32 TLB entries
  - Double-precision IEEE-754 floating point co-processor (GRFPU)
- Internal on-chip high speed AMBA (AHB) bus
- Instruction trace and AMBA (AHB) trace buffers for debugging
- Timer unit with four 32-bit timers including watchdog
- Secondary timer unit with four 32-bit timers
- Primary and secondary interrupt controller for 31 interrupts
- On-chip 192 KiB memory block with EDAC
- External memory support with error correction and detection:
  - Bus width: 8 bits, or 32 bit data plus 8/16 bits for EDAC checkbits, 24 bit address
  - 8 bit BCH EDAC for SRAM and PROM, 16 bit Reed-Solomon EDAC for SDRAM
  - Memory types: SRAM, SDRAM, PROM / EEPROM / NOR-FLASH and I/O address space
  - Programmable wait-states:
    - SRAM read/write cycle 2 - 5 clock cycles
    - PROM / EEPROM / NOR-FLASH read cycle 2 - 32 clock cycles
    - One idle cycle between accesses to SRAM and PROM
- Debug Support Unit (DSU) accessed via JTAG or SpaceWire RMAP targets
- Two SpaceWire ports with RMAP targets, maximum 200 Mbps full duplex data rate
- Configurable I/O selection matrix, connecting a subset of the available I/O units to 67 pins:
  - Four SpaceWire ports, maximum 200 Mbps full duplex data rate
  - Redundant MIL-STD-1553B BRM (BC/RT/BM) interface
  - Two CAN 2.0B bus controllers
  - Six UART ports, with 8-byte FIFO
  - Ethernet MAC with RMII 10/100 Mbps port
  - SPI master serial port
  - I2C master serial port
  - ASCS16 (STR) serial port
  - SLINK 6 MHz serial port
  - CCSDS / ECSS Telecommand decoder (five input channels), maximum 10 Mbps input rate
  - CCSDS / ECSS Telemetry encoder, maximum 50 Mbps output rate
  - 26 input and 38 input/output general purpose ports


CONTACT INFORMATION

Aeroflex Gaisler AB
Kungsgatan 12
411 19 Göteborg
Sweden

Tel: +46 31 7758650
Fax: + 46 31 421407

Sales contact:
sales@gaisler.com
www.aeroflex.com/gaisler