AGGA-3 in an Avionic System

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ABSTRACT

The AGGA-3 (Advanced GPS/GALILEO ASIC) is a radiation-tolerant, low power consumption new generation GNSS baseband ASIC. The AGGA-3 includes a GNSS baseband processor, the LEON-FT fault-tolerant microprocessor with its powerful IEEE-754 compliant FPU (GRFPU), an FFT module, UART's, a SpaceWire module, containing four SpaceWire interfaces and a DSU SpW interface. The digital hardware and its interfaces are highly flexible, which makes this component useful for a wide range of applications ranging from platform positioning to Earth observation such as radio occultation, scatterometry and precise orbit determination in support of radar interferometry.
In an application the AGGA-3 will receive the incoming navigation signal from an AD converter. Via SpaceWire or UART interfaces the AGGA-3 can be connected to the Onboard Computer.
The ASIC will be manufactured by Atmel in ATC18RHA technology.

1. INTRODUCTION

The AGGA-3 (Advanced GPS/GALILEO ASIC) is a radiation-tolerant, low power consumption new generation GNSS baseband ASIC. As a further development of the AGGA-2 (Advanced GPS/GLONASS ASIC), the AGGA-3 is initiated within the Earth Observation Preparatory Programme (EOPP) of ESA to support Earth observation (EO) applications of navigation signals. It is a digital integrated circuit providing all the high-speed digital signal processing functionality for precise GNSS applications.

The AGGA-3 includes all the functionality of the AGGA-2 except for the GLONASS signal demodulation capability. It furthermore includes new powerful features and flexibility of the modules, which will allow GNSS space equipment developers to focus on application algorithms and software. The AGGA-3 takes advantage of a number of other European technical developments such as the LEON processor and SpaceWire developments. In addition, the understanding of signal processing optimal for atmospheric sounding has been improved from experience with GRAS and Lagrange receivers. With the future availability of the modernized GPS and Galileo signals, additional measurements of enhanced quality are possible.

The objective of the AGGA-3 development is to update the AGGA family with state-of-the-art technologies and signal processing techniques. This will enable more compact, low power consumption Radio-Occultation (RO) and Precise Orbit Determination (POD) instruments for various planned ESA EO missions, yet providing improved (GNSS) signal processing techniques. Moreover, the AGGA-3 chip will allow for miniaturized receivers and support numerous different applications. Although developed for Earth science applications, thanks to its flexibility, the AGGA-3 chip can be used for operational applications such as spacecraft attitude determination, PVT determination in LEO, GEO and launchers, etc.

The second part of this article will describe the AGGA-3 in general, with special attention to the external interfaces. The third part will address how the AGGA-3 can be applied and the fourth part will present AGGA-3 ASIC features.

2. AGGA-3 DESCRIPTION

2.1 General

The AGGA-3 consists mainly of the On-chip processor modules around the LEON core, the GNSS module and the interface modules.

A high-level overview of the AGGA-3 device is given in the following figure.

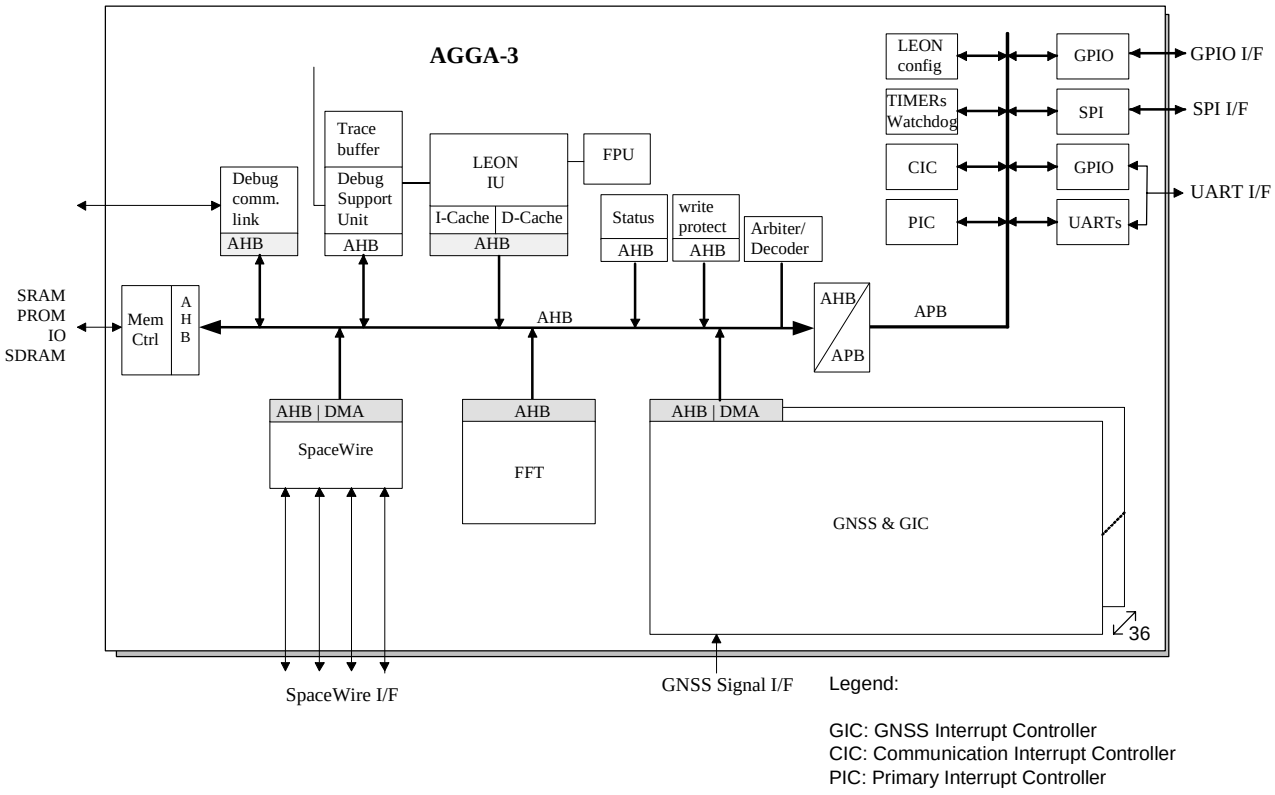

Figure 1: Overview of the AGGA-3 device

2.2 On-Chip Processor Modules

The LEON processor implements the SPARC V8 standard as defined in the SPARC V8 architectural manual. The LEON processor and periphery consist of:

- a cache sub-system,
- a memory controller
- interrupt controller,
- two UARTS,
- two 24-bit timers,
- one 24-bit watchdog,
- an AHB status register,
- a write protection unit,
- a watch point registers,
- and a 16-bit I/O-port.

AMBA AHB/APB buses are used to connect the processor to the peripheral devices and the other modules. The Floating Point Unit (FPU) implemented in AGGA-3 is the GRFPU from Gaisler Research.

The memory interface can use 8-, 16-, 32-, and 39-bit memories with common or separate write strobes.

2.3 GNSS Module

The GNSS baseband processor is capable of processing the current and future GPS signals L1 C/A, L2C, L5, P(Y) and the open access Galileo signals that have shift register based codes and BOC(n,n) subcarrier. It includes digital down-conversion, beam-forming, enhanced power level detection, code and carrier loop aiding support, and optimized raw sampling for open-loop signal tracking. Codeless tracking of GPS L2 P(Y) signals is supported. Implementation losses are reduced thanks to 3-bit pre-correlation processing. Functional blocks usually located in software have been included in hardware with a high flexibility to accelerate the signal processing of the new GPS and Galileo wideband signals and to increase the number of processed signals. 36 highly configurable single-frequency GNSS channels are available. Each channel includes 5 complex code correlators, a dual integration stage for data, decryption or secondary code stripping, a secondary code sequencer, and a carrier and code aiding unit. The data from the GNSS baseband processor is transferred to memory by direct memory access (DMA).

The GNSS module is connected to the AMBA bus via two interfaces: the AHB master and the AHB slave interface. The AHB master interface is required to implement DMA capability to the GNSS module and the AHB slave interface is used to access all module internal registers (read and write).

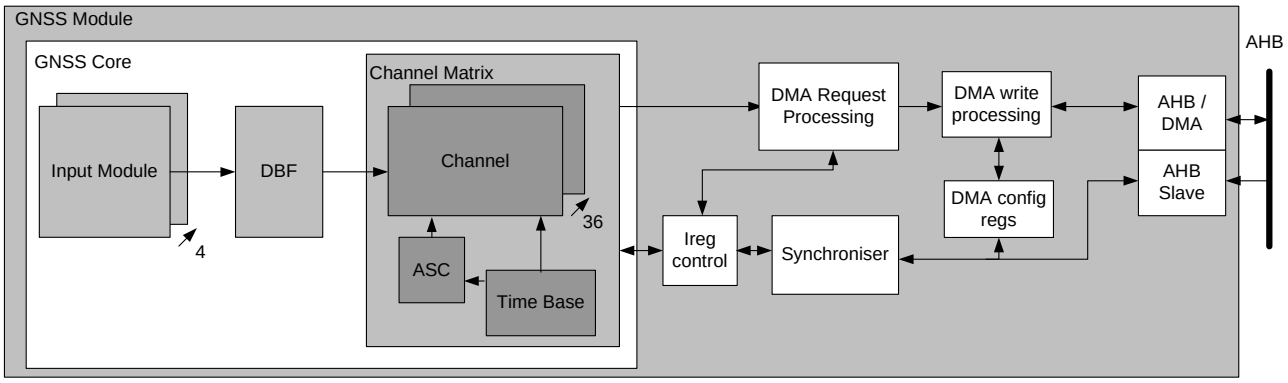

Figure 2: GNSS module

2.4 Main AGGA-3 External Interfaces

The following main external interfaces are provided by the AGGA-3.

DMA Controller
The AGGA-3 provides DMA (Direct Memory Access) from the GNSS module to the external memory via AMBA bus and memory controller. DMA requires to be a bus master and to get the ownership of the AMBA bus. The DMA controller requests the bus from the arbiter and releases the bus after completion of the transfers. In the meantime no other bus master can do any transfer via the AMBA bus.
The DMA controller is implemented following a de-centralised approach as shown in Figure 3. This means that a DMA controller is directly implemented inside the GNSS module. This DMA controller can only provide DMA capability from the GNSS module.

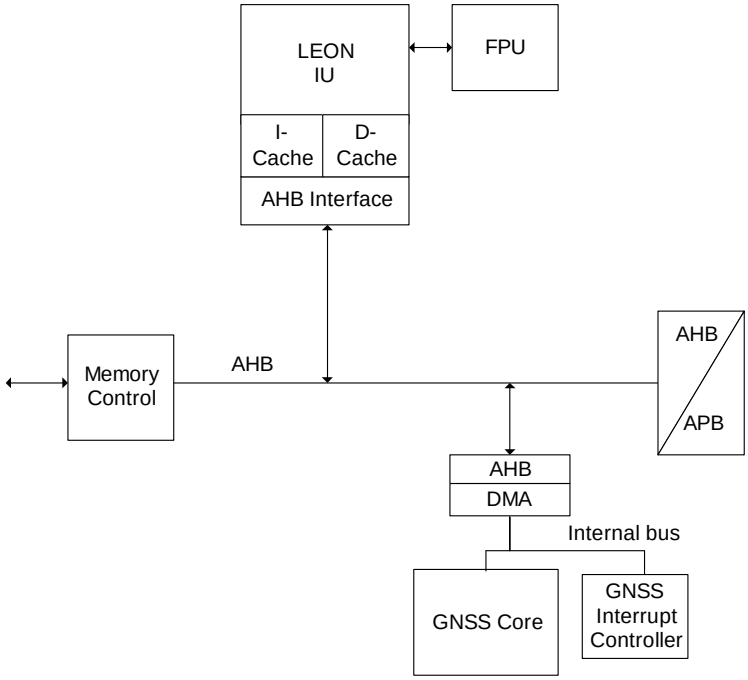

Figure 3: De-centralised DMA controller

Modules connected to AMBA AHB and their accessibility:

Module	Master	Slave	DMA	AHB-Priority
LEON-Integer Unit	x			0
Debug Comm. Link	x			3
GNSS module	via DMA	x	x	2
SpaceWire module	via DMA		x	1
FFT module		x		
Memory Controller		x		
AHB/APB Bridge		x		
Debug Support Unit		x		
Status Register		x		
Write protect		x		
Total:	4	7		

Table 1: AMBA AHB connections

UARTS

Two UARTs are implemented in the AGGA-3. Their design is based on that provided by the LEON on-chip peripherals. However, the original LEON UARTs have only a single byte interface for transmission and reception. This leads to high interrupt rates if high communication bandwidth is required. In AGGA-3 two 16 byte FIFOs are implemented per UART, one in receive and one in transmit direction.

The receive FIFO of the UART (from serial to parallel) generates one additional interrupt, if its status changes to half full.

The transmit FIFO of the UART (from parallel to serial) also generates one additional interrupt, if its status changes to half empty. Each of the additional interrupt sources can be masked off, the information is provided by status flags, as well.

Since data transmission via the DSU-UART is not interrupt driven, its design remains unchanged.

SpaceWire interfaces

There are two different kinds of SpaceWire interfaces inside the AGGA-3 device. One SpaceWire interface is directly connected to the Debug Support Unit (DSU), and the other SpaceWire interfaces are connected via an AHB interface. They are implemented for general communication purposes.

The electrical interface of the SpaceWire links is single-ended and the maximum data rate per SpaceWire link is around 30 Mbit/s.

DSU SpaceWire interface

The DSU SpaceWire interface is implemented parallel to the DSU UART. The purpose for the DSU SpaceWire interface is to support software download and to decrease the booting time through the higher data rate in comparison with an UART. Both serial interfaces, the DSU UART and the DSU SpaceWire use a common AHB interface to get access to the AHB bus.

The UART or the SpaceWire can be used alternatively. The one which should be selected is controlled by an external select signal. If the SpaceWire interface is disabled, the data and strobe output signals are in high impedance (tri-state) and the data and strobe input signals are mute. This function allows the implementation of a bus structure topology at board level connecting several AGGA-3 devices.

The DSU SpaceWire interface uses the same protocol as the one used with the DSU communication link (UART). Through the DSU SpaceWire link read or write transfers can be generated to any address on the AHB.

Communication SpaceWire interface

The AGGA-3 provides four SpaceWire interfaces (or channels) for communication purposes.

The four communication SpaceWire links share a common AHB interface and a common DMA controller. Data can be transferred via DMA from a SpaceWire link to the external memory and vice versa. The DMA function requires that the SpaceWire-AHB interface has the capability to become AHB master.

The registers used to control the SpaceWire interface are split into two groups. One group contains all registers commonly used by the SpaceWire interface. The other group contains all registers which are individual to each SpaceWire channel.

Common used registers:

- Time interface control registers

Channel dependent registers:

The SpaceWire frontend is programmed by the following registers:

- Control and Status Register
- Test Register.

In addition to the SpaceWire frontend registers there are 6 further registers to support DMA for each link, three registers to control receive and three registers to control transmit direction. To configure transmit and receive direction, a common configuration register is used.

Receive direction: - Receive start address register
- Receive end address register
- Receive current address register

Transmit direction: - Transmit start address register
- Transmit end address register
- Transmit current address register

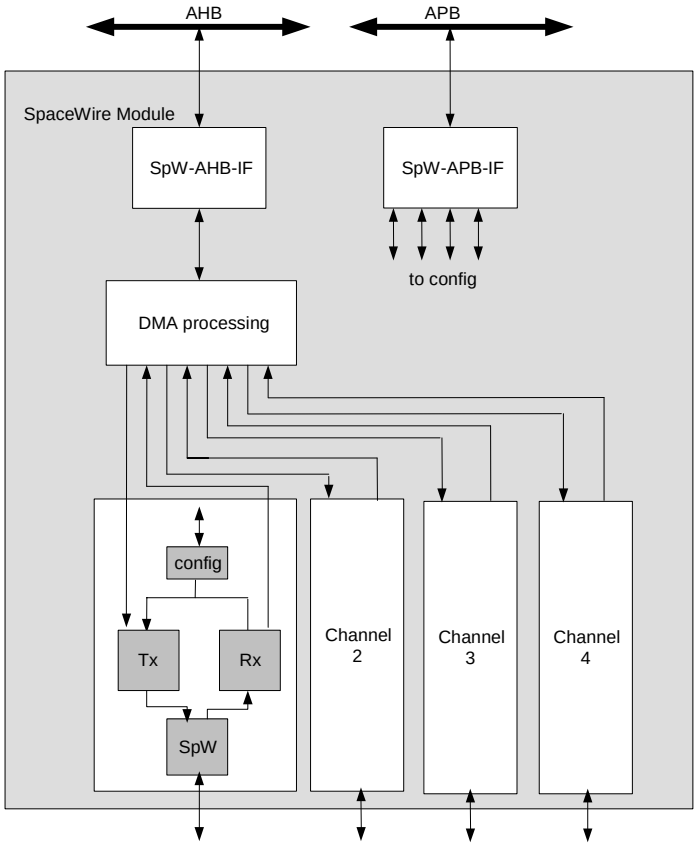

Figure 4: SpaceWire module

Serial Peripheral Interface (SPI)

The SPI module works as SPI master, but it is prepared to operate either as Clock Master or as Clock Slave. The data to transmit are received from the processor in the *spi_tx_reg*, when this register is empty. Then, if the *start* signal is activated, the data in *spi_tx_reg* is loaded into the shift register. The *ss_n* of the corresponding slave is asserted (low active), the SCKM is enabled and the data sent through MOSI. The number of bits to send is programmable with *spi_bits_to_send*.

When the transmission of the data is finished, two different actions are taken:

- If *clk_phase* = 1, the *ss_n* can remain activated during consecutive data transfers and the SCKM is disabled. Then, if *start* is still activated and the *spi_tx_reg* is not empty, the process begins again.
- If *clk_phase* = 0, or start = 0 or even *spi_tx_reg* is empty, the *ss_n* is deactivated and the SCKM is disabled, going to the initial state.

The serial data at MISO are received in a shift register bit by bit, until it is full. Then the data is loaded into the *spi_rcv_reg* and *RCV_FULL* signal is activated to be read from the processor.

Additional General Input and Output Ports

In addition to the 16 bit I/O port provided by the LEON on-chip peripherals, further 16 general purpose input/output ports are implemented. All 16 GPIOs are implemented as bi-directional ports. This gives the user the possibility to configure the number of inputs or outputs according to his needs. The operation of the general purpose input and output port is programmed through the following registers:

- direction register
- data register

The direction register controls the mode of the bi-directional pin (input or output). The data register provides write access to the pins configured as outputs and read access to the signal status of the pins configured as inputs. Read access to pins configured as output results in the output status set at the most recent write access.

3. APPLICATION OF THE AGGA-3

In a typical environment the AGGA-3 receives the incoming down-converted navigation signal from an Analogue/Digital converter (ADC). 32 input pins are provided by the AGGA-3 ADC interface for the incoming signals. A synchronization signal can be generated by the AGGA3 in order to synchronize the ADC data stream with the internal baseband signal processing clock. Additionally, the results of the power level measurements inside the AGGA-3 can be used to establish an Automatic Gain Control (AGC) loop. The AGC adapts the RF gain and thus controls the saturation degree of the ADC. Despreading of the navigation signal is performed in the signal processing part of the chip. Tracking loops closed by software executed on the LEON processor allow for code and carrier phase measurements and navigation data demodulation. The results are transmitted via SpaceWire to the Onboard Computer (OBC), which also controls the AGGA-3 using the same SpaceWire connection. Alternatively, the communication between the AGGA-3 and the OBC can also be handled by means of the UARTs. The main data bus inside the AGGA-3, the AHB bus, can be connected to an external memory via the Memory controller.

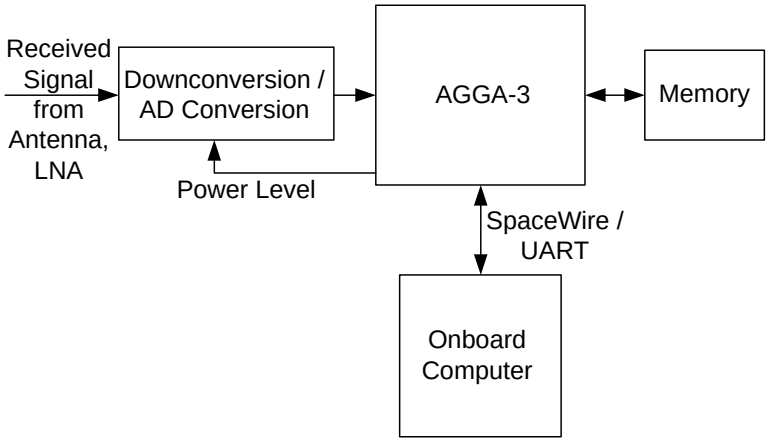

Figure 5: AGGA-3 typical application

4. AGGA-3 ASIC DESCRIPTION

The AGGA-3 chip will be manufactured by Atmel in the ATC18RHA technology. The assumed package for the AGGA-3 device is an Atmel MQFP package with 352 pins.
The GNSS part of the AGGA-3 chip runs at max. 40 MHz and the LEON part runs at max. 80 MHz.

5. CONCLUSION

The AGGA-3 is under development at Astrium GmbH and Austrian Aerospace under ESA guidance. This chip provides enhanced high-speed digital signal processing functionality, a powerful on-chip microprocessor and versatile interfaces for a wide range of GNSS applications. The powerful features and flexibility of AGGA-3, which takes advantage of a number of other developments (LEON, SpaceWire,..) and experience from on-going programmes (Earth observation missions, Galileo,..), will allow GNSS space equipment developers to focus on increasingly complex application algorithms and software.

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