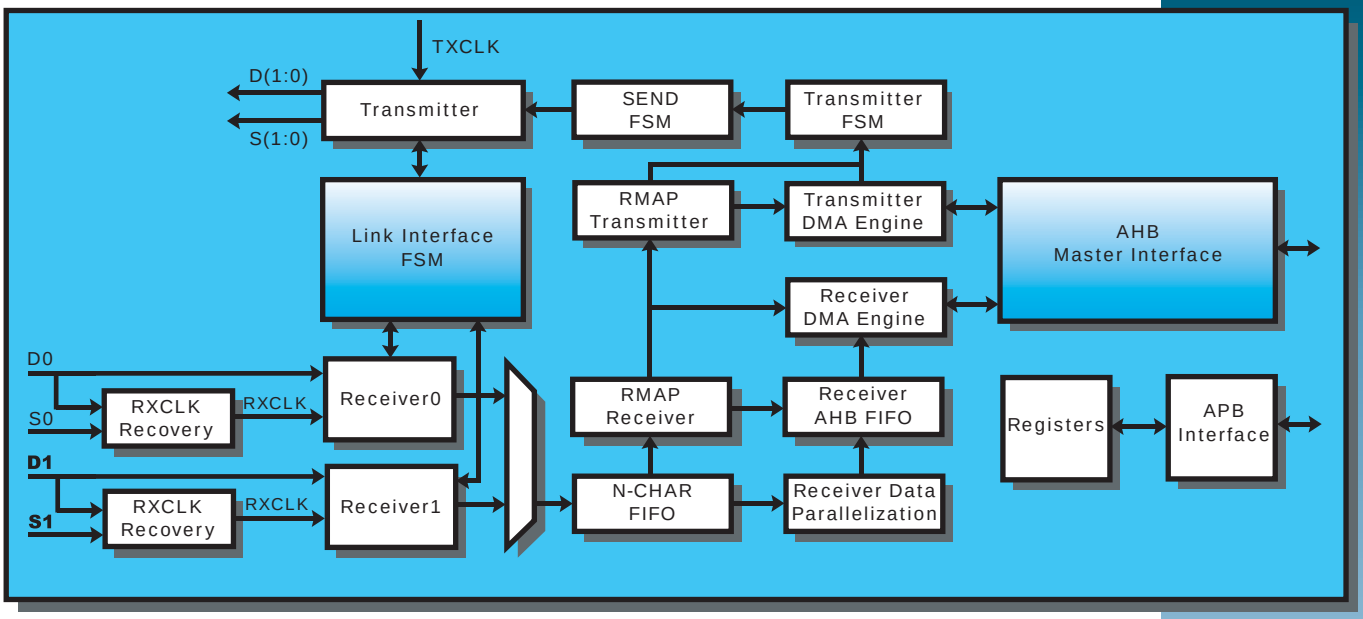
GRSPW2
SpaceWire Node Interface

AEROFLEX GAISLER

Description

The GRSPW2 core implements a SpaceWire node interface with RMAP target and AMBA host interface. The core complies to the SpaceWire standard (ECSS-E-ST-50-12C), the protocol identification extension (ECSS-E-ST-50-51C) and the RMAP protocol (ECSS-E-ST-50-52C). Receive and transmit data is autonomously transferred between the SpaceWire node interface and the AMBA AHB bus using DMA transfers. Through the use of receive and transmit descriptors, multiple SpaceWire packets can be received and transmitted without processor involvement. The GRSPW2 control registers are accessed through an AMBA APB interface. For critical space applications, a fault-tolerant (FT) version of GRSPW2 is available with full SEU protection of all RAM blocks. GRSPW2 is the successor to the GRSPW with additional features.



The GRSPW2 is inherently portable and can be implemented on most FPGA and ASIC technologies. The table below shows the approximate Cell/LUT count and frequency for eight different GRSPW2 configurations on Actel RTAX, RT ProASIC3, Xilinx Virtex5 and ASIC technologies.

Size and Performance

RTAX: C-Cells, R-Cells, RAM blocks, AMBA 60 MHz, SpW 200Mbit/s
RT ProASIC3: Versa Tile Cells, RAM blocks, AMBA 45 MHz, SpW 150Mbit/s
Virtex5: LUTs, Registers, RAM blocks, AMBA 130 MHz, SpW 400Mbit/s
ASIC: gates

Core configuration	RTAX	RTProASIC3	Virtex5	ASIC
GRSPW2	2,800 / 1,400 / 3	5,800 / 5	1,800 / 1,400 / 3	15,000
GRSPW2 + RMAP (1)	4,100 / 1,700 / 4	8,500 / 6	2,700 / 1,700 / 4	20,000
GRSPW2 + 2P (2)	2,900 / 1,500 / 3	6,100 / 5	1,800 / 1,500 / 3	15,000
GRSPW2 + 4DMA (3)	3,600 / 1,800 / 3	7,400 / 5	2,200 / 1,800 / 3	19,000
GRSPW2 + RMAP + 2P + 4DMA	5,100 / 2,200 / 4	10,200 / 6	3,300 / 2,100 / 4	26,000
GRSPW2-FT (4)	2,900 / 1,400 / 5	6,000 / 10	1,900 / 1,400 / 5	15,000
GRSPW2-FT + RMAP (4)	4,200 / 1,700 / 6	8,500 / 12	2,800 / 1,700 / 6	21,000
GRSPW2-FT + RMAP + 2P + 4DMA (4)	5,100 / 2,200 / 6	10,400 / 12	3,400 / 2,200 / 6	26,000

(1) Includes the RMAP target, (2) Dual SpaceWire ports, one is available in the standard configuration.
(3) Four DMA Channels, one is available in the standard configuration, (4) Fault-tolerant version.

Features:	• Full implementation of SpaceWire standard ECSS-E-ST-50-12C • Protocol ID extension ECSS-E-ST-50-51C • Optional RMAP protocol ECSS-E-ST-50-52C • AMBA AHB back-end with DMA • Descriptor-based autonomous multi-packet transfer • Low area and high frequency • SEU protection fault-tolerance • Portable design • 4,200 Cells on RTAX2000S FPGA, 15,000 ASIC gates • 200 Mbit/s on RTAX2000S FPGA, 400 Mbit/s on ASIC • Netlist delivery • Configurable with one or two SpaceWire ports
Improvements:	• Up to four DMA Channels • Support for RMAP error code 12 • Supports faster SpaceWire clocks • Simpler configuration • Supports multiple logical adresses and ranges
Benefits:	• Tested and verified against several other SpaceWire cores • Low area and high frequency • Easily portable between FPGA and ASIC • Low-cost project license • SEU protection of all RAM blocks
Deliverables:	• FPGA/ASIC netlist or VHDL source code • Stand-alone testbench • Optional plug&play interface for GRLIB IP Library • User's Manual • Driver for RTEMS, VxWorks and Linux

CONTACT INFORMATION

Aeroflex Gaisler AB
Kungsgatan 12
411 19 Göteborg
Sweden

Tel: +46 31 7758650
Fax: + 46 31 421407

Sales contact:
sales@gaisler.com
www.aeroflex.com/gaisler