GR-VPX-GR740-BOARD

Development Board

User's Manual

Intentionally Blank

Table of Contents

List of Figures

List of Tables

1 Introduction

1.1 Scope of the Document

This document provides a User's Manual and Interface document for the "GR-VPX-GR740-BOARD" Development and Demonstration board.

The work has been performed by Cobham Gaisler AB, Göteborg, Sweden.

1.2 Reference Documents

[RD1] GR740, "Data Sheet and User's Manual",Cobham Gaisler, GR740-UM-DS, available from http://www.gaisler.com/index.php/products/components/GR740

[RD2] GRMON3 User's Manual, available from: https://www.gaisler.com/index.php/products/debug-tools/grmon3

[RD3] GR-VPX-GR740 Board_schematic.pdf, Schematic

[RD4] GR-VPX-GR740 Board_assy_drawing.pdf, Assembly Drawing

2 Abbreviations

ASIC	Application Specific Integrated Circuit.
DSU	Debug Support Unit
EDAC	Error Detection and Correction
EDCL	Ethernet Debug Communication Link
ESD	Electro-Static Discharge
GPIO	General Purpose Input / Output
IC	Integrated Circuit
I/O	Input/Output
IP	Intellectual Property
LDO	Low Drop-Out
LVDS	Low Voltage Digital Signalling
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
POL	Point of Load
PPS	Pulse Per Second
PROM	Programmable Read Only Memory
SOC	System On a Chip
SP3T	Single Pole,3-throw (position) Switch
SPW	SpaceWire
TBC	To Be Confirmed
TBD	To Be Defined

3 Board Introduction

3.1 Overview

This document describes the *GR-VPX-GR740* Development Board.

This equipment is a 1 slot, 6U high board with a VPX backplane format, consists of

- Main Board: *GR-VPX-GR740*
- Mezzanine Board: GR-VPX-SPW-MEZZ

The GR-VPX-GR740 board shown in Figure 3-1 integrated with a 6U front panel and a mezzanine board, which can be used stand alone on the bench top, or installed in a VPX rack.

A GR-VPX-SPW-MEZZ mezzanine board has been developed and integrated with the GR-VPX-GR740, which provides two SpaceWire interface from the GR740 to the Front panel.

This board provides developers with a convenient hardware platform for the evaluation and development of software.

Note: The delivered product is GR-VPX-GR740 main board and GR-VPX-SPW-MEZZ mezzanine board, the mezzanine board only provides two SpaceWire interfaces in the front panel.

This user manual provides information about the GR-VPX-GR740 main boards many different mezzanine interfaces through out the document, such descriptions are provided in order to help the users to develop their own mezzanine board, for example see section 4.6 Mezzanine Interfaces. However, the delivered GR-VPX-SPW-MEZZ do not implement all such interfaces and only provides two SpaceWire interfaces in the front panel.

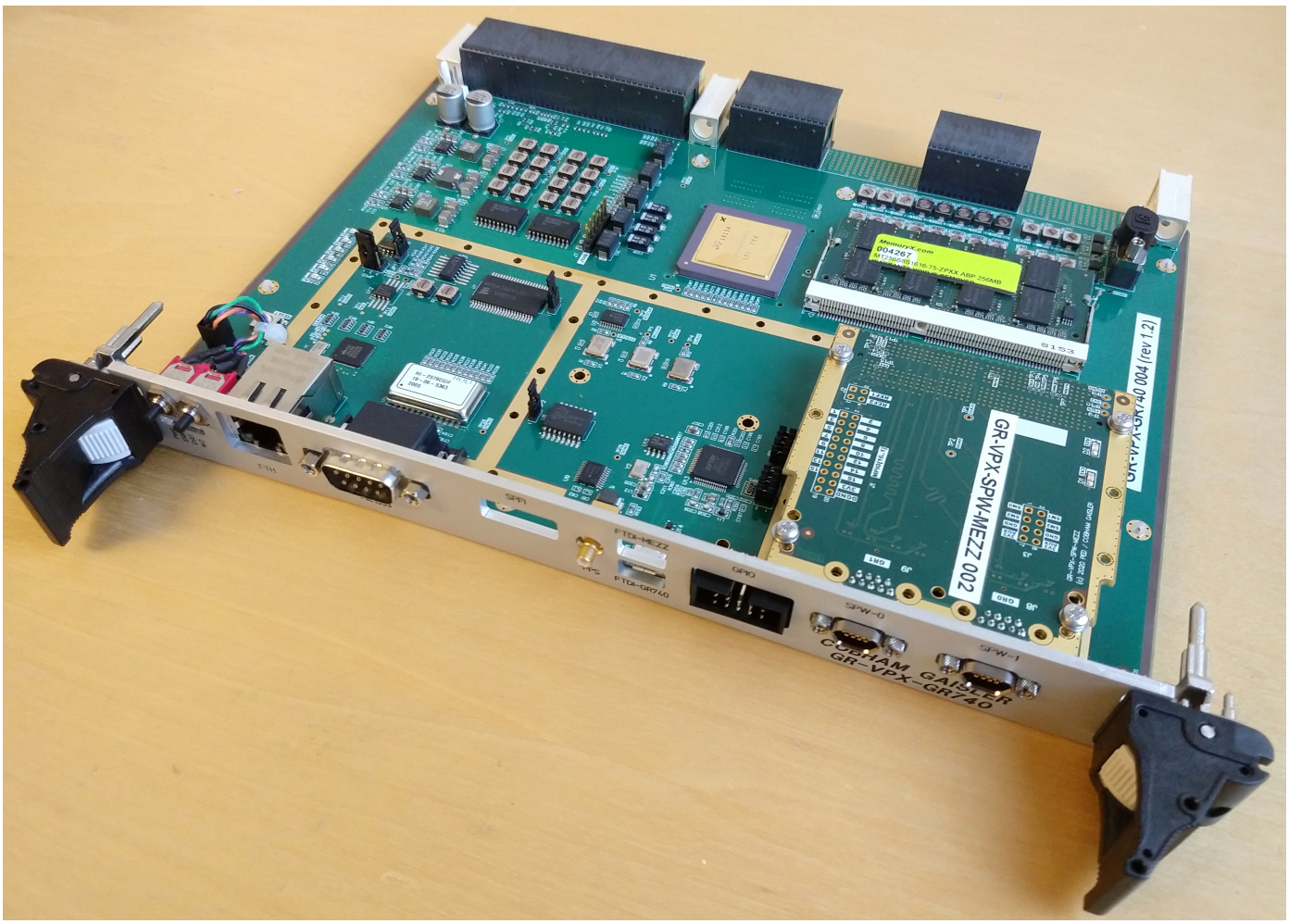

Figure 3-1: GR-VPX-GR740 Development Board mounted with GR-VPX-SPW-MEZZ mezzanine board

The board contains the following main items as detailed in section 4 of this document:

Main Board

- size 233.35x160mm
- Cobham Gaisler GR740 radiation-hard system-on-chip featuring a quad-core fault-tolerant LEON4 SPARC V8 processor
- 1 Mbit (128k x 8bit) MRAM
- 512 Mbit SPI memory (Cypress, S25FL512SAGN in SOIC-16 package)
- SODIMM socket for SDRAM memory (48 bit wide interface)
- Gbit Ethernet interface with standard RJ45 connector
- Dual MIL-1553 Interface
- 1 PPS interface
- FTDI Serial to USB converter for JTAG and UART interface
- Front Panel General Purpose IO interface
- FMC style 400 pin mezzanine connector
- VPX Backplane interface
- VIN power input (+5V to +12V) via backplane or 2 pin header
- on-board regulators converting from VIN to 3.3V, 2.5V & 1.2V
- switches for bootstrap and configuration settings

Mezzanine Board

- GR-VPX-SPW-MEZZ
  - 2 SpaceWire interfaces connected to the GR740 router (Port 1 and 2)

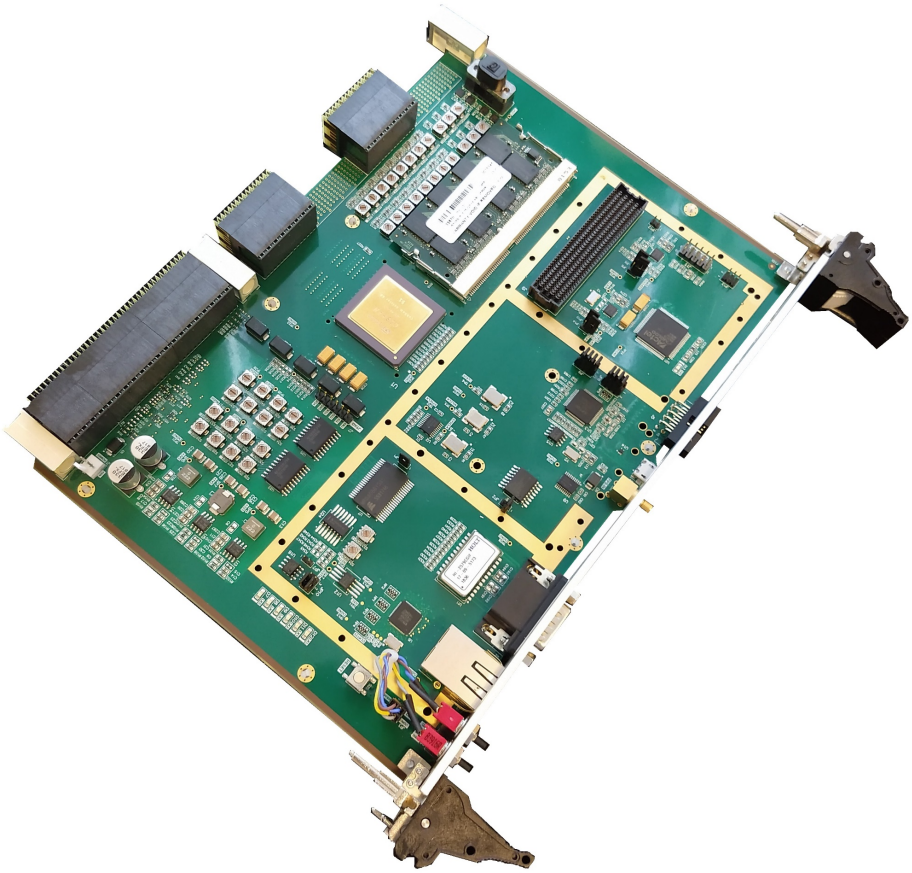

Figure 3-2: GR-VPX-GR740 Main Board without mezzanine board

3.2 Handling

ATTENTION: OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an unpowered state.

When operating the board in a 'stand-alone' configuration, the power supply should be current limited to prevent damage to the board or power supply in the event of an over-current situation.

This board is intended for commercial use and evaluation in a standard laboratory environment, nominally, 20°C. All devices are standard commercial types, intended for use over the standard commercial operating temperature range (0 to 70ºC).

4 Board Design

4.1 Board Block Diagram

The *GR-VPX-GR740* Board provides the electrical functions and interfaces as represented in the block diagram, Figure 4-1.

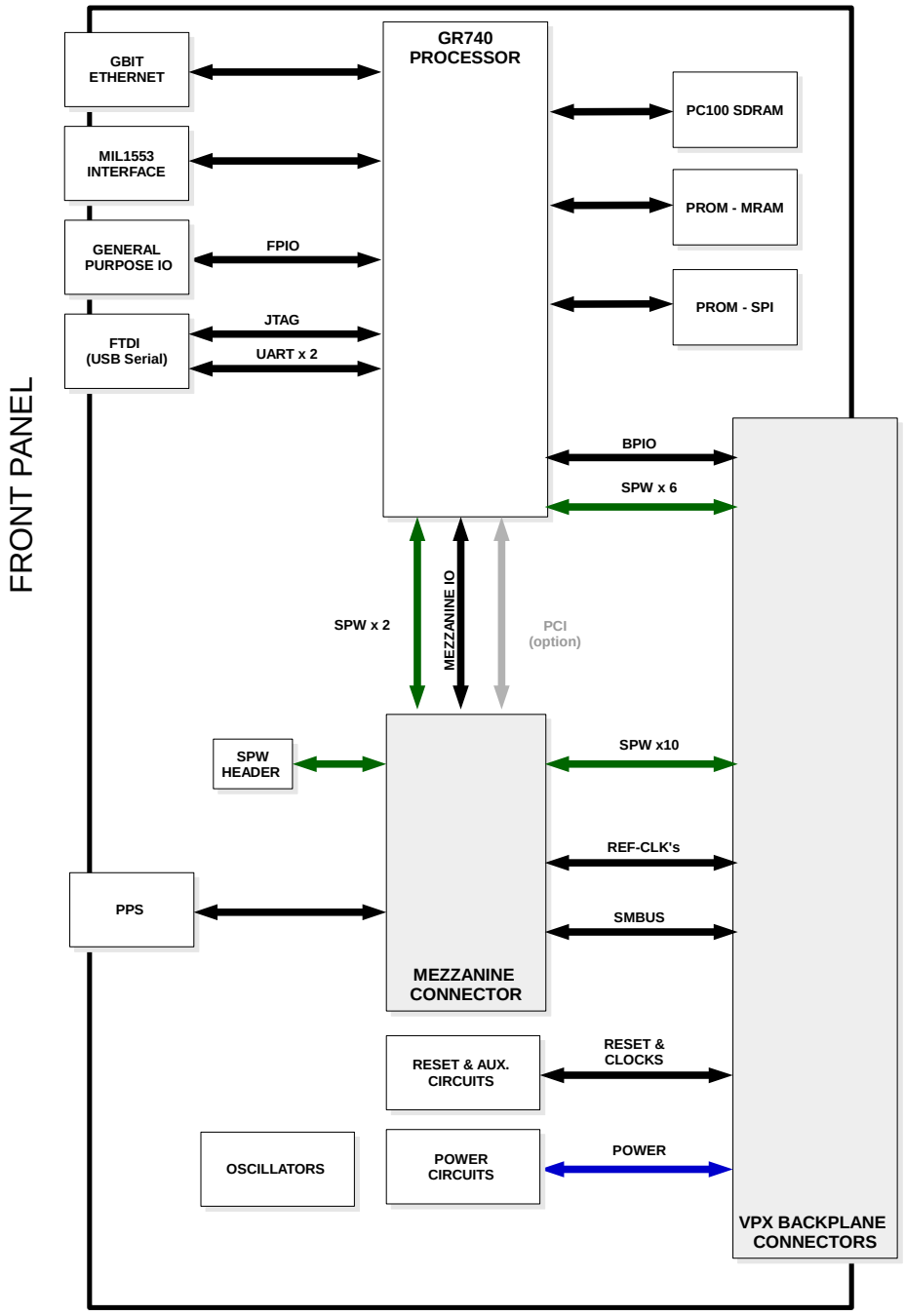

Figure 4-1: GR-VPX-GR740 Board Board Block Diagram

The Mezzanine connector of the *GR-VPX-GR740* is a FMC High Pin Count (400 pin) connector conforming to the VITA57.1 format.

The *GR-VPX-SPW*-MEZZ board has been designed to mount on this connector and provides the electrical functions and interfaces as represented in the block diagram, Figure 4-2.

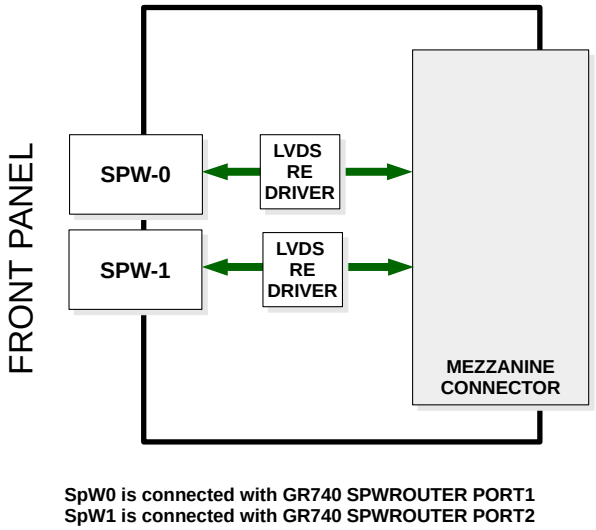

Figure 4-2: GR-VPX-SPW-MEZZ Mezzanine Board Block Diagram

4.2 Board Mechanical Format

The design is conceived as a 6U high, 1 slot (25.4mm) wide module for mounting in the controller slot of a 6U rack with a VPX Backplane.

The dimensions of the main PCB are 233.35x160mm (excluding the connector protrusions).

To ensure boards are correctly installed in the appropriate slot of a backplane, the VPX backplane standard defines mechanical alignment keys (Figure 4-3) which can be defined with various orientations of keying.

However, as the keying for the backplane itself is not definitively known at this stage, this board has been equipped with 'universal' keys (Part number TE-1-1469492-9), allowing its installation into any slot. These keys can easily be dismounted and replaced with specific key parts if when these are known.

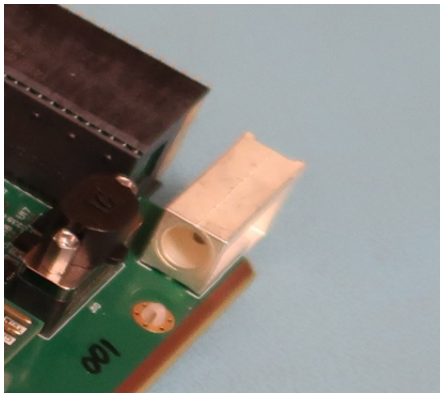

Figure 4-3: VPX Style mechanical keying

This prototype board is intended for installation in a rack with forced air cooling. However, for installation in conduction cooled environment, a future design could accommodate standard wedge locks on the top and bottom rail edges of the board.

This would require the exact wedge lock type and mounting hole definition to be known, and the front panel to be modified to accommodate them.

A standard FMC style (VITA 57.1) mezzanine interface connector allows the Mezzanine board to be mounted to the main board.

The dimensional format, outline and mezzanine connector position for the Mezzanine board follows the requirements of VITA57.1 for a double-slot conduction cooled board.

Due to the necessity to be able to fit the SDRAM module and power converters on the mezzanine board, the back edge of the board has been extended, giving an overall size of 139 x 117.5mm.

The face to face mounting distance of the two boards is 10mm. While the prototype board is mounted using simple 10mm nickel-brass Hex spacers, a future design could accommodate a custom aluminium bracket to act as a thermal interface between the two boards.

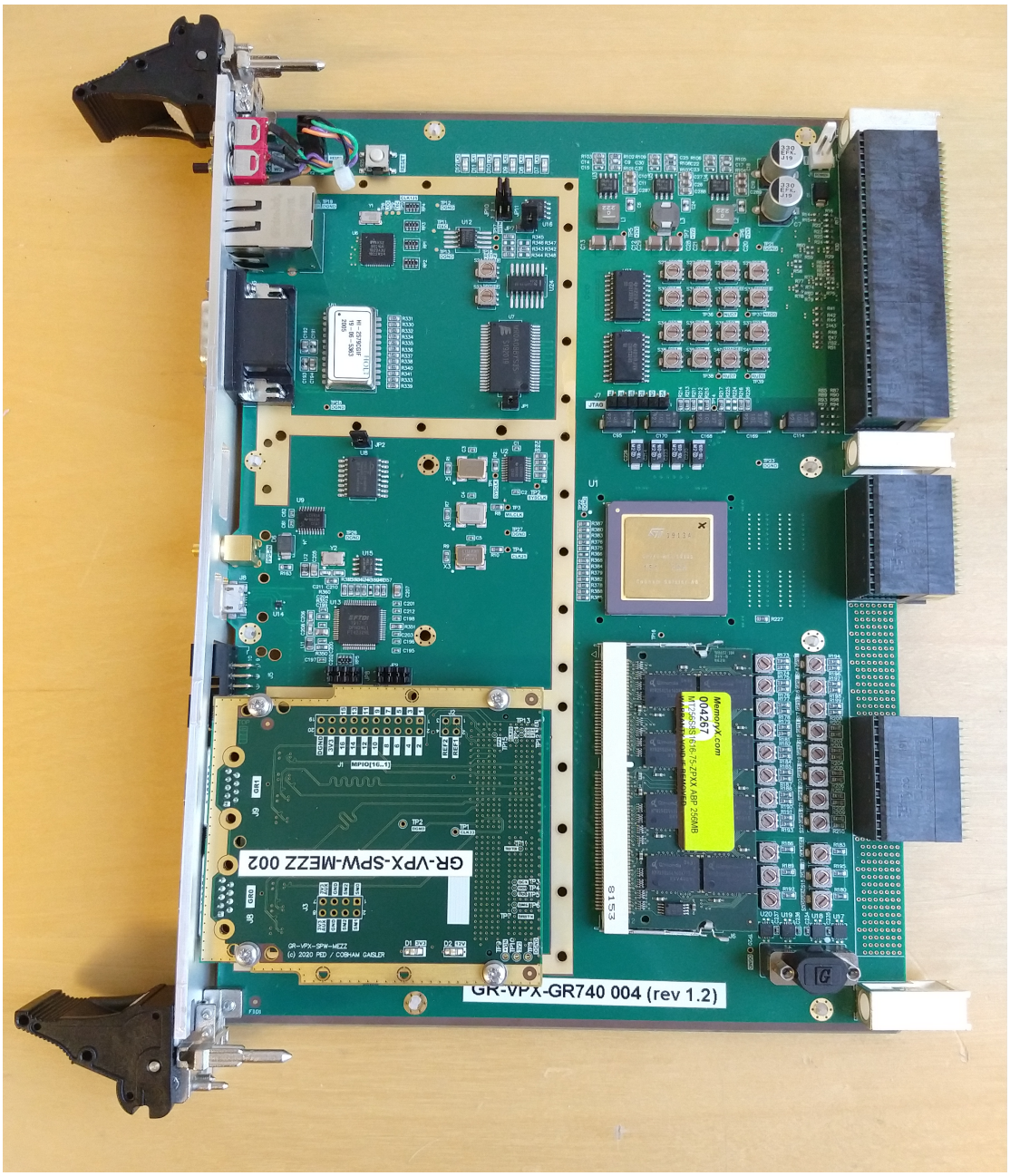

Figure 4-4: Mezzanine board mounted on a GR-VPX-GR740 main board

4.3 GR740 Microcontroller

The *GR740 Leon Processor* is a complex device with many modes of operation. For the details of the interfaces, operation and programming, refer to [RD1].

4.4 Memory

These boards incorporate various on-board memories as follows:

Main Board

SODIMM -SDRAM An SODIMM Module with 48 bit wide interface to the GR740 with 32 bit data and 16 bit check-bit memory width.

MRAM – PROM An MRAM based, 8 bit wide boot Prom is connected to the Prom interface of the GR740. The implemented device is an *Everspin MR0A08B*, which is a 128k x 8bit, 3.3V device. This device is pin compatible with and alternative device from *3D plus: 3DMR1M08VS1426.*

SPI Flash 512 Mbit SPI serial boot prom (Cypress, S79FL512S). The SPI boot memory is connected directly to the SPIM interface of the GR740 Micro-controller. S79FL256S consists of two SPI devices internally. Clock and chip select is common for the two internal chips bus the MOSI/MOSI buses are independent. IO0..IO3 versus IO4..IO5. Only the first data bus is connected with the GR740 and the GR740 has only one SPI bus. The consequence is that only half the device capacity can be used. Hence S79FL512S is used to get 32 MiB capacity.

4.5 Main Board Interfaces

4.5.1 SPW Interfaces

The board incorporates a large number of SpaceWire Links distributed between the VPX backplane, GR740 Processor, mezzanine connector, External Front panel connectors and an on board header/connector.

The on-board SPW network is represented in the figure below.

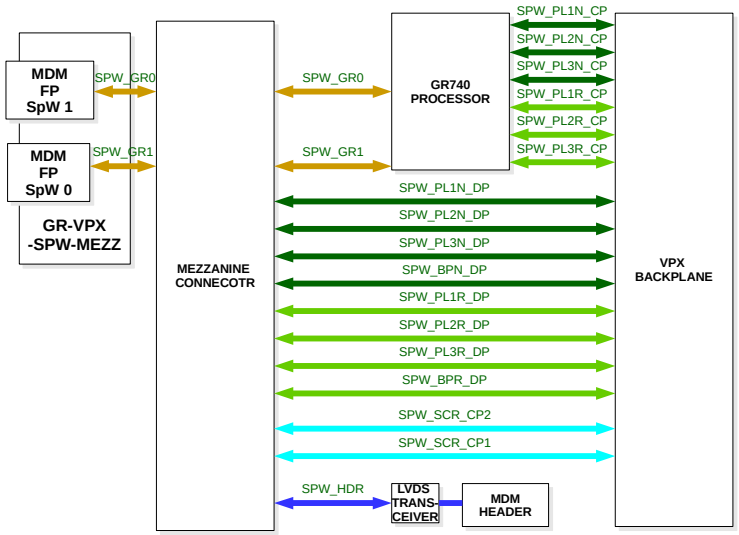

Figure 4-5: On-Board Spacewire Connections

GR740 SPW router port number	Front panel SpW interface
PORT 1	Front Panel port marked as SpW-0
PORT 2	Front Panel port marked as SpW-1

Table 1: GR740 SpW Router Port mapping to Front panel interfaces

GR740 SPW router port number	Backplane SpW Interface
PORT 3	SPW_PL1R_CP
PORT 4	SPW_PL2N_CP
PORT 5	SPW_PL3R_CP
PORT 6	SPW_PL2R_CP
PORT 7	SPW_PL1N_CP
PORT 8	SPW_PL3N_CP

Table 2: GR740 SpW Router Port mapping to Backplane interfaces

The *SPW_0 and SPW_1* link connect to MDM9S connector on the *GR-VPX-SPW-MEZZ* board and is buffered with a *DS10BR150* LVDS repeater circuits.

The *SPW_HDR* link connect to an MDM9S connector on the *GR-VPX-GR740* board and is buffered with a *DS10BR150* LVDS repeater circuits.

4.5.1.1 SPW connector implementation details and precautions to follow

This equipment has SPW ports that use Low Voltage Differential Signalling (LVDS) which has limited common mode voltage protection.

Before plugging the SPW cable between two equipment's please power up and make sure that there is no voltage difference between their grounds.

The SPW standard specification specifies that the cable side outer-shield is bonded to the connector shell, but does not say anything about the grounding/bonding of the connector side shell. In this equipment the SPW connector side shell are by default bonded to the front panel/box local chassis but not bonded to the local GND of the SPW circuits.

The pin three of this equipment's SPW connectors are connected to the GND through a parallel capacitor (100p) and resistor (10k) network. When connected to a SPW cable (properly designed as per the standard) the pin three will be connected to its inner shield. Note the inner shield does not provide end to end ground connection between two equipment's as per the SPW standard.

In this equipment there is no grounding provided via the SPW connectors (neither through pin three inner shield nor through connector side shell between two equipments). The users connecting the board to other equipment only via SPW should ensure grounding via other means (e.g. a dedicated wire).

4.5.2 Ethernet

An Ethernet RJ45 interface is provided on the board front panel, and is connected to the Ethernet interface of the *GR740 processor.* This interface can operate in either 100Mbit or Gbit mode, and can be used either for standard networking, or if the GR740 is configured, can be used for a debug communication link over Ethernet (EDCL).

An external PHY, (*Micrel KSZ9021GN*) is implemented on the board.

4.5.3 MIL-1553

A dual MIL-1553 interface is provided on the board, with a DSUB 9 pin connector (J3) on the front panel. The interface is connected to the MIL-1553 interface pins of the *GR740,* via a *Holt HI-2579* transceiver. This is a CMOS dual transceiver with integrated transformers designed to meet the requirements of the MIL-STD-1553 / MIL-STD-1760 specifications.

The configuration on the board is intended for 'transformer coupling'. For a 'direct coupling' interface to external equipment external 55 Ohm series resistors would be

have to be added externally. If necessary for the configuration being used, external parallel termination may have to be added.

4.5.4 PPS

An SMB connector is available on the front panel. This signal is terminated with a 50 Ohm load and buffered. The PPS signal input is inverted by the buffer and driven as PPS_IN and PPS_IN2. The PPS_IN is interfaced with the mezzanine connector, which can be used by the mezzanine board to process the input and output PPS_OUT signal which is also available from the mezzanine connector.

A jumper option on the board, *JP10*, allows to select PPS_IN2 (unprocessed PPS) or PPS_OUT (processed PPS) to be driven to the GPIO0 of GR740 and distributed over the backplane as a differential signal on the AUXCLK_OUT pins.

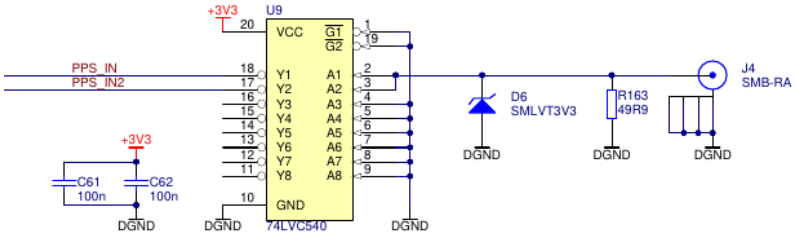

Figure 4-6: PPS input circuitry

4.5.5 FTDI (USB Serial)

An FTDI FT4232 serial to USB interface chip is implemented on the board to allow an external PC to interface to the following serial interfaces

- *GR740* JTAG DSU interface

- *GR740* UART-0 serial interface

- *GR740* UART-1 serial interface

The front panel interface connector is a standard USB Micro-AB style connector.

4.5.6 VPX Backplane

The design is required to support several different backplane routing schemes with prime and redundant SPW connections over the Data Plane and Control planes.

This requires many resistors to be installed or removed depending on which configuration is required to be implemented. For details, refer to the schematic diagrams [RD3].

4.6 Mezzanine Interfaces

Note: The delivered product is GR-VPX-GR740 main board and GR-VPX-SPW-MEZZ mezzanine board, the mezzanine board only provides two SpaceWire interfaces in the front panel.

This section provides information about the GR-VPX-GR740 main boards many different mezzanine interfaces, such descriptions are provided in order to help the users to develop their own mezzanine board. The delivered GR-VPX-SPW-MEZZ do not implement all listed interfaces below and only provides two SpaceWire interfaces in the front panel.

The Mezzanine connector is a FMC High Pin Count (400 pin – Female) connector conforming to the VITA57.1 format.

- HPC-400 FMC connector
- 2 SpaceWire interfaces connected to the GR740 router (Port 1 and 2)
- 2 Thin Pipes routed to P1 on the back edge (used for 2 SpaceWire interfaces)
- 2 Fat Pipes and 4 Half Pipes routed to P3 and P5 on the back edge
- 1 SpaceWire interface to on-board MDM9S connector (SPW-HDR)
- PPS
  - Input from the Front-panel
  - Output to the backplane as AUXCLK_OUT
- CLK25 – 25 MHz clock from an oscillator on board as input to the mezzanine board
- Additional backplane clocks
  - REFCLK_OUT from the mezzanine can be connected to a LVDS transmitter onboard the GR-VPX-GR740, the LVDS output is connected to backplane signal REF-CLK.
  - REF-CLK1 and REF-CLK2 connected to the backplane (Differential LVDS in or out, must be driven as needed form the mezzanine board)
- SMBUS to VPX backplane
- Power to mezzanine circuits (+12V nominal)
- 9 General purpose I/O from the GR740 (MPIO signals 1 – 9)
  - Note the GPIO (MPIO) signals are also shared with bootstrap functionality (see Table 6).
- *RESETN* from main board reset circuit
- *SYSCON#* and *SYSCONP#* from VPX backplane

- PCI interface (32-bit) from the GR740
  - The PCI_HOSTN signal for the GR740 is pulled HIGH in the GR-VPX-GR740. The PCI_HOSTN is also connected to the mezzanine from where this signal can be driven low to make the GR740 as Initiator/Master PCI interface.
  - The PCI_INTA, PCI_INTB, PCI_INTC and PCI_INTD are pulled high in the GR-VPX-GR740.
  - The PCI GNT signal is pulled high in the GR-VPX-GR740, this signal must be driven low by the mezzanine board, since the PCI interface between GR740 and the mezzanine board is a point to point interface. The GNT can be permanently tied to low in the mezzanine board to let GR740 always initiate the PCI communication.
  - The PCI clock must be provided from the mezzanine board.
  - The PCI specification requires that the following system signals are pulled-up PCI_FRAME, PCI_STOP, PCI_PAR, PCI_IRDY, PCI_PERR, PCI_TRDY, PCI_SERR and PCI_DEVSEL. These signals must be pulled up in the mezzanine board.

4.7 GPIO

30 general purpose I/O pins of the GR740 processor are used in this design for various signalling purposes as listed in the table below.

These General purpose I/O pins are 3.3V LVCMOS voltage levels.

- *GPIO* refers to 'General Purpose I/O pins' of the GR740 processor, accessed through the GPIO1 registers (0xFF902000 – 0xFF9020FF) of the GR740.
- *GPIO2* refers to 'General Purpose I/O pins' of the GR740 processor, accessed through the GPIO2 registers of the GR740.
- *FPIO* refers to 'Front Panel I/O' pins which are connected to the front panel connector J5
- *MPIO* refers to 'Mezzanine I/O pins' which are signals connecting between the GR740 and the mezzanine connector.
- *BPIO* refers to 'Back Plane I/O pins' which allows some signals to be used for signalling between slots on the back panel, depending on various switches as listed in the table.

No over-voltage protection components are included on the front panel FPIO signals of the *GR-VPX-GR740 Board* board. The signals are connected from the microprocessor via 330 Ohm resistors, to the front panel. The limiting resistors provide a basic level of protection case of unintended S/C at the input pins. However, care must be taken to ensure that any external circuitry connected does not exceed the allowable voltage limits for the input/output pins.

GR740 Pin	Signal Name	Function
GPIO0	PPS_GR740	*PPS* input to GR740
GPIO1	MPIO1	GPIO to mezzanine connector
GPIO2	MPIO2	GPIO to mezzanine connector
GPIO3	MPIO3	GPIO to mezzanine connector
GPIO4	MPIO4	GPIO to mezzanine connector
GPIO5	MPIO5	GPIO to mezzanine connector

GR740 Pin	Signal Name	Function
GPIO6	MPIO6	*GPIO to mezzanine connector*
GPIO7	MPIO7	GPIO to mezzanine connector
GPIO8	MPIO8	GPIO to mezzanine connector
GPIO9	MPIO9	GPIO to mezzanine connector
GPIO10	FPIO0	Front panel J5
GPIO11	FPIO1	Front panel J5
GPIO12	FPIO2	Front panel J5
GPIO13	FPIO3	Front panel J5
GPIO14	FPIO4	Front panel J5
GPIO15	FPIO5	Front panel J5

Table 3: Functions assigned to GPIO signals of GR740

Pin	Function	Connects to
GPIO2_0	BPIO0	*SCN-PL1N-SE-UD1* if BPIO6='0' and S26 = (C-3) *SCN-PL1N-FP-UD1* if BPIO6='0' and S26 = (C-1) *SCN-PL1R-SE-UD1* if BPIO6='1' and S34 = (C-3) *SCN-PL1R-FP-UD1* if BPIO6='1' and S34 = (C-1) For Switch configuration (C-3) and (C-1), refer section 5.1.1
GPIO2_1	BPIO1	*SCN-PL1N-SE-UD2* if BPIO6='0' and S27 = (C-3) *SCN-PL1N-FP-UD2* if BPIO6='0' and S27 = (C-1) *SCN-PL1R-SE-UD2* if BPIO6='1' and S35 = (C-3) *SCN-PL1R-FP-UD2* if BPIO6='1' and S35 = (C-1)
GPIO2_2	Not available as GPIO	
GPIO2_3	Not available as GPIO	
GPIO2_4	Not available as GPIO	
GPIO2_5	Not available as GPIO	
GPIO2_6	BPIO2	*SCN-PL1N-SE-UD3* if BPIO6='0' and S28 = (C-3) *SCN-PL1N-FP-UD3* if BPIO6='0' and S28 = (C-1) *SCN-PL1R-SE-UD3* if BPIO6='1' and S36 = (C-3) *SCN-PL1R-FP-UD3* if BPIO6='1' and S36 = (C-1)
GPIO2_7	BPIO3	*SCN-PL1N-SE-UD4* if BPIO6='0' and S29 = (C-3) *SCN-PL1N-FP-UD4* if BPIO6='0' and S29 = (C-1) *SCN-PL1R-SE-UD4* if BPIO6='1' and S37 = (C-3) *SCN-PL1R-FP-UD4* if BPIO6='1' and S37 = (C-1)
GPIO2_8	Not available as GPIO	
GPIO2_9	Not available as GPIO	
GPIO2_10	Not available as GPIO	
GPIO2_11	BPIO4	*SCN-PL1N-SE-UD5* if BPIO6='0' and S30 = (C-3) *SCN-PL1N-FP-UD5* if BPIO6='0' and S30 = (C-1) *SCN-PL1R-SE-UD5* if BPIO6='1' and S38 = (C-3) *SCN-PL1R-FP-UD5* if BPIO6='1' and S38 = (C-1)
GPIO2_12	FPIO6 if SP3T switch S23 is set to (C-3)	Front panel J5
	BPIO5 if SP3T switch S23 is set to (C-1)	*SCN-PL1N-SE-UD6* if BPIO6='0' and S31 = (C-3) *SCN-PL1N-FP-UD6* if BPIO6='0' and S31 = (C-1) *SCN-PL1R-SE-UD6* if BPIO6='1' and S39 = (C-3) *SCN-PL1R-FP-UD6* if BPIO6='1' and S39 = (C-1)
GPIO2_13	FPIO7 if SP3T switch S24 is set to (C-3)	Front panel J5
	BPIO6 if SP3T switch S24 is set to (C-1)	BPIO6 controls
GPIO2_14	Not available as GPIO	
GPIO2_15	Not available as GPIO	

Table 4: Functions assigned to GPIO2 signals of GR740

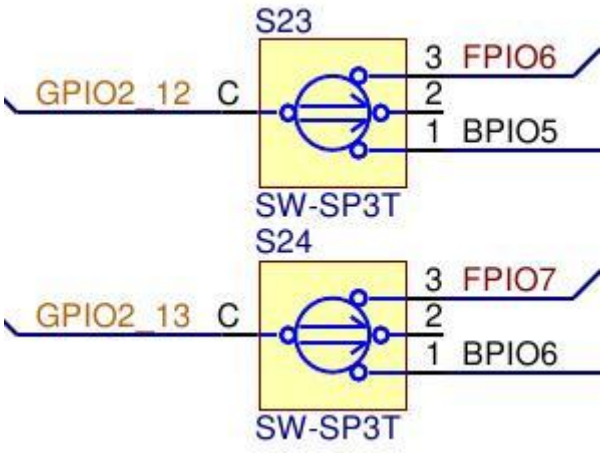

Figure 4-7: Configuration option for switch S23 and S24

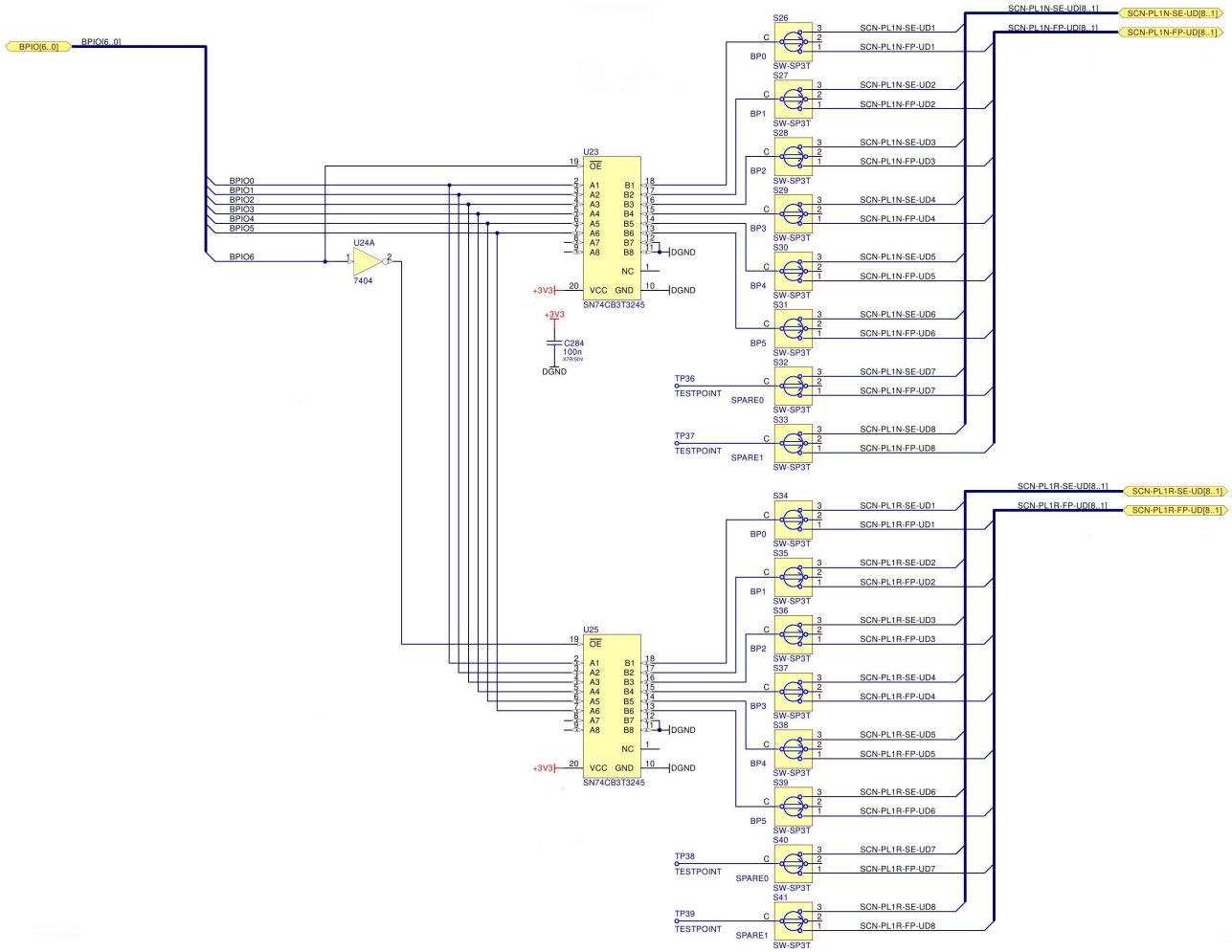

Figure 4-8: Configuration option for switch S27 to S41

4.8 Debug Support Unit Interfaces

Program download and debugging to the GR740 processor is performed using the GRMON Debug Monitor tool from Cobham Gaisler ([RD2]). The GR740 processor provides an interface for Debug and control of the processor by means of a host terminal via its DSU interface, as represented in Figure 4-9.

Three control signals and a data connection from the Debug Support Unit interface to the processor:

DSUEN: This signal is connected to SP3T switch S5. When the switch is set to '1' DSU debugging is enabled.

The signal can be pulled low with switch S5 to disable the DSU. Switching off the DSU also sets the clock gating to off for all the debug interfaces (SpaceWire, JTAG and Ethernet interfaces connected to debug subsystem).

DSUBRE: The front panel push-button switch pulls the DSUBRE signal high to force the processor to halt and enter DSU mode.

DSUACT: When the processor is halted, the front panel LED will illuminate

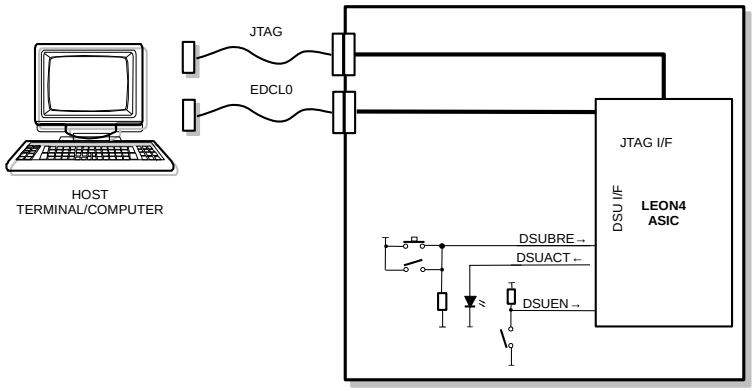

Figure 4-9: Debug Support Unit connections

To communicate with the processor, two possibilities for the data connection to the processor are provided:

JTAG-DCL JTAG Debug Communication Link (6 pin connector header J7 or using the FTDI interface connector J8 if the jumpers JP8 1-2,3-4,5-6 and 7-8 are installed).

EDCL Ethernet Debug Communication Link (front panel RJ45 connector J3)

For more information, please refer to [RD2].

4.9 Oscillators and Clock Inputs

The oscillator and clock scheme for the *GR-VPX-GR740 Board* Board is shown in Figure 4-10. On this board, all oscillators are soldered to the PCB.

A single 50 MHz oscillator is buffered and split to drive the following clocks:

- SYS_CLK of GR740
- SPW_CLK of GR740
- MEM_CLK of GR740
- FPGA_CLK – auxiliary clock provided to Mezzanine connector

A dedicated 20 MHz oscillator provides the MIL1553 clock for the GR740.

The *GR740 g*enerates the *SD_CLK* for the SDRAM using internal logic.

For more details of the internal PLL structure and clock gating features of the *GR740*, please refer to the Data Sheet and User Manual of GR740.

A dedicated 25 MHz oscillator provides an optional clock for the REF_CLK output to the backplane. Alternatively, the REF_CLK output can instead be configured with a jumper to be generated by the FPGA on the Mezzanine. This clock output is converted to a differential LVDS output.

The AUX_CLK is a differential LVDS output which can be generated either as a copy of the 1PPS input pulse, or via a jumper from an output of the FPGA on the mezzanine.

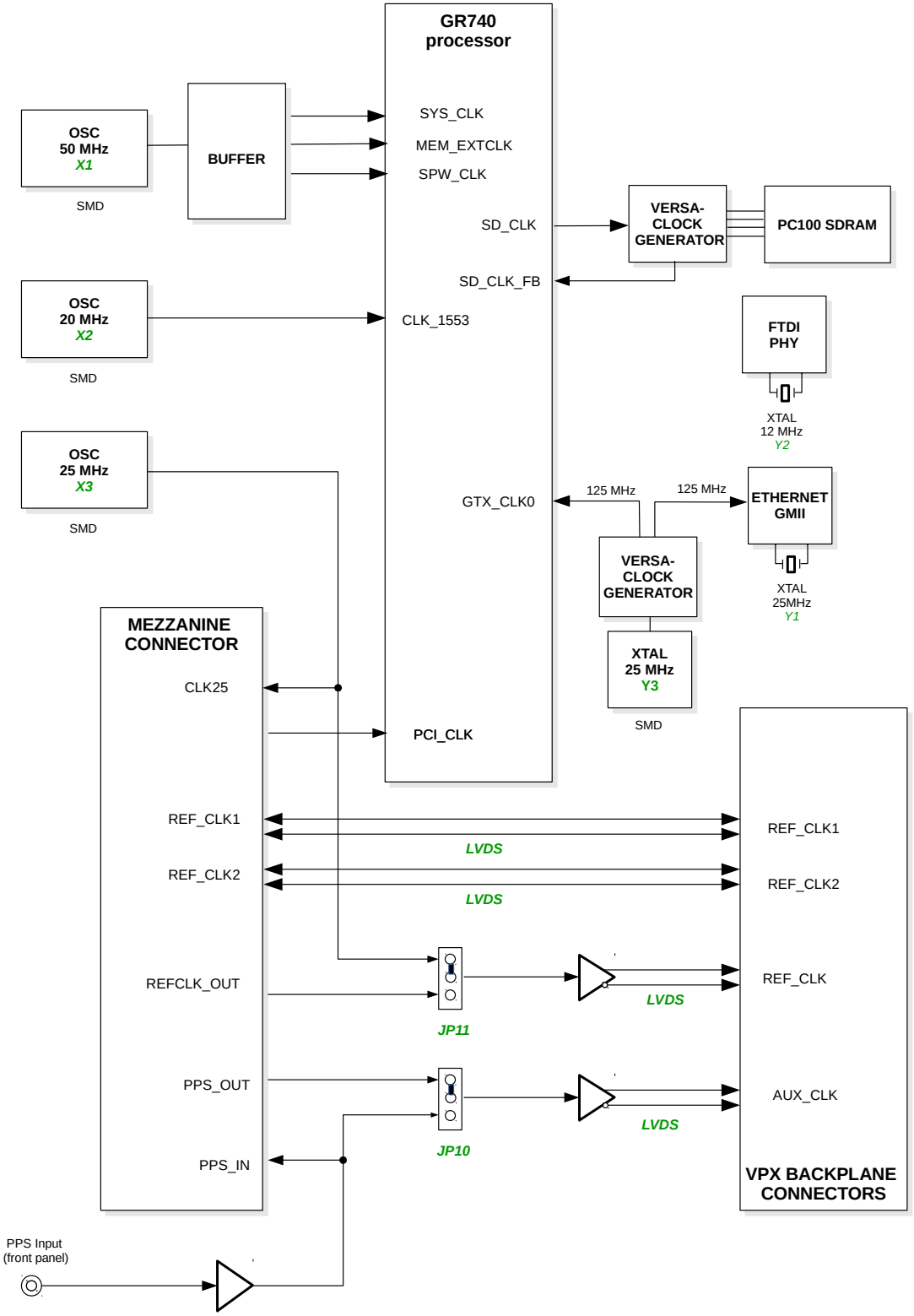

Figure 4-10: Board level Clock Distribution Scheme – GR-VPX-GR740

4.10 Power Supply and Voltage Regulation

The power configuration scheme implemented on the *GR-VPX-GR740* board is represented in Figure 4-11.

Power at a nominal input voltage of +12V can be provided from the VS1 input connections of the backplane, or in stand-alone mode from a dedicated 2-pin header on the board.

On-board 5A DCDC buck regulators (*TI, TPS54527DDA)* generate the following voltages:

+3.3V (VIO for GR740 and peripherals)

+2.5V (VIO for GR740-LVDS)

+1.2V (Vcore for GR740)

These regulators accept a wide input range from 5V to 15V.

For the board, the nominal supply input is considered to be +12V, but in stand alone operation can also be powered from a +5V supply. The maximum limit is +14.5V due to the 15V transient protection diode at the input.

The initial design considered an output current of 2A on each output. However, the Buck regulators and components are dimensioned for a capability of 5A, to provide margin.

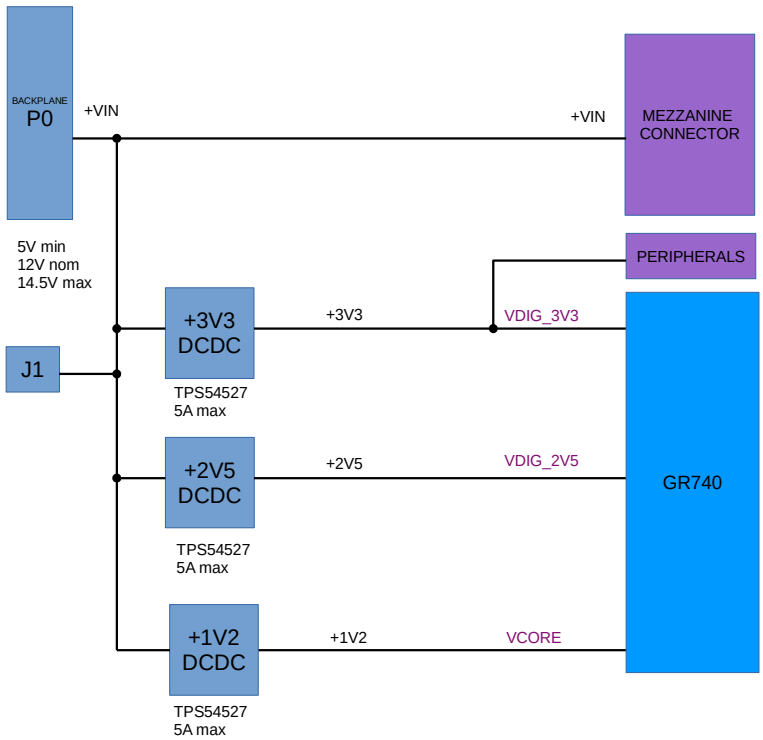

Figure 4-11: Power Regulation Scheme – GR-VPX-GR740

The mezzanine board can receive power at a nominal input voltage of +12V provided from the *12P0V* pins of the mezzanine connector.

5 Setting Up and Using the Board

The board is provided with a default configuration set by bootstrap settings.

For additional information, refer to [RD1], and for information about the Bootstrap signals, refer to section 5.1.

To operate the board stand alone on the bench top, install the power configuration jumpers appropriately, and a power supply in the range +5V to +12V to the board connector J1.

ATTENTION! To prevent damage to board, please ensure that the Figure 4-11 correct power supply voltage and polarity is used with the board.

Do not exceed +14.5V at the power supply input, as this may damage the board.

The PWR LED on the front panel should be illuminated indicating that the power supply is present and the board is generating the supply voltages that it requires.

To perform program download and software debugging on the hardware it is necessary to use the *Cobham Gaisler GRMON3* debugging software, installed on a host PC (as represented in Figure 4-9). Please refer to the GRMON3 documentation for the installation of the software on the host PC (Linux or Windows), and for the installation of the associated hardware dongle.

To perform software download and debugging on the processor, a link from the Host computer to the DSU interface of the board is necessary. As described in section 4.8 this is achieved via the FTDI USB interface.

Program download and debugging can be performed in the usual manner with GRMON3. More information on the usage, commands and debugging features of GRMON3, is given in the GRMON3 Users Manuals and associated documentation, [RD2].

5.1 Switches and Bootstrap Signals

A number of features of the board have configuration options which need to be set correctly in order for the boards to operate correctly.

This includes:

- GR740 Bootstrap signals

- VPX Backplane Configuration switches

These signals and their meaning are listed below, together with the suggested default configuration

5.1.1 SP3T Switch description and configuration properties

As shown in Figure 5-1 below the SP3T switches can be set in three different positions.

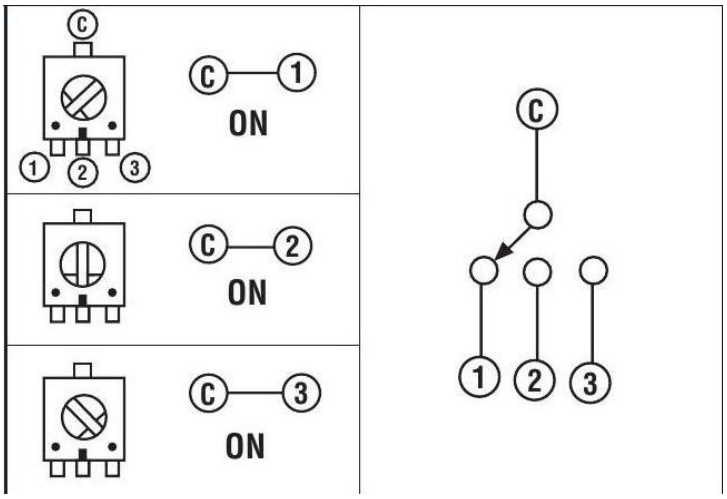

Figure 5-1: SW-SP3T configuration options and schematics.

The image below provides the mapping between the schematics and a switch implemented onboard.

Figure 5-2: SW-SP3T mapping between schematics and a switch onboard

There are forty SP3T configuration switches available onboard. The switch schematics and mapping provided in Figure 5-2 remains the same on all those switches, irrespective of the position or the naming convention of the switch.

5.1.2 GR740 Bootstrap Signals

The schematics below shows the configuration available for switch S1 to S22.

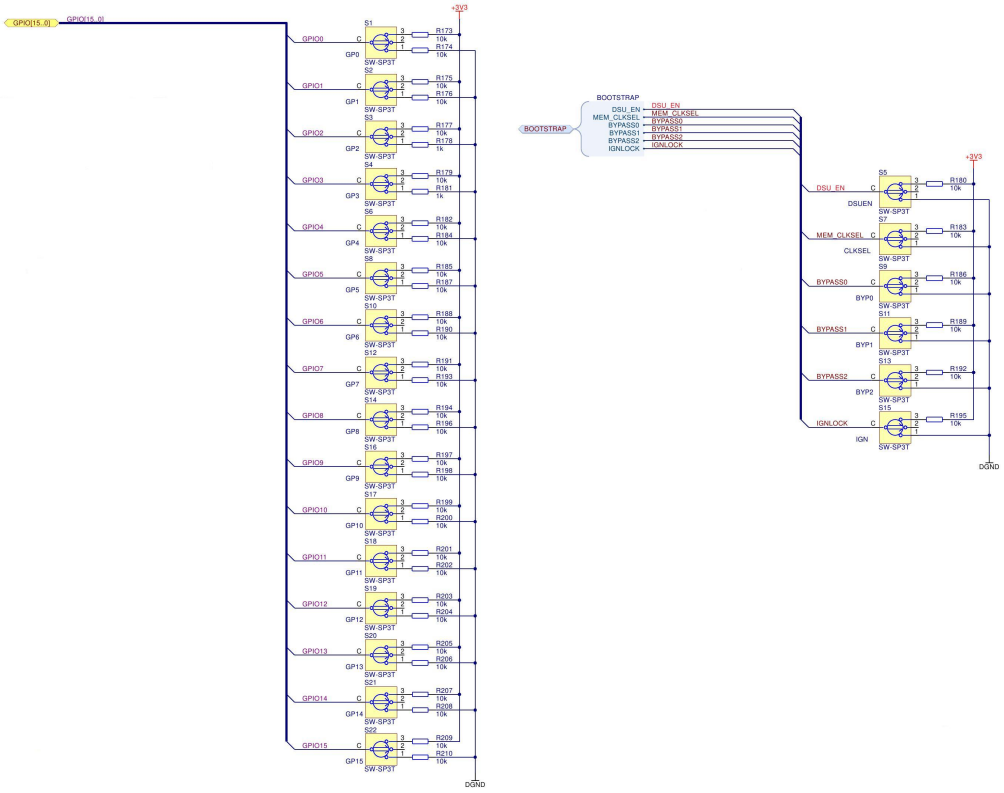

Figure 5-3: Configuration options for switch S1 to S22

These signals are set using the Single pole 3 position miniature switches. These switches can be set with a fine-bladed screwdriver. These 3 position switches have the possibility to set the signal value to 'pull-up' (='high') (C-3), 'float' (='undefined') (C-2), or 'pull-down (='low') (C-1).

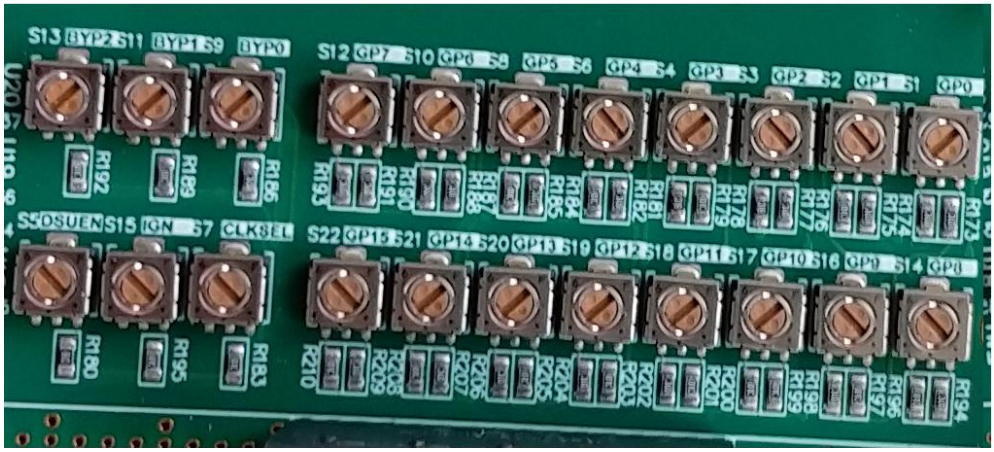

Figure 5-4: GR740SBC Bootstrap Signals default configuration

Signal	Function	Switch	Default
DSUEN	Debug Support Unit Enable	S5	High (C-3)
MEM_CLKSEL	Select source for Memory clock	S7	High (C-3)
BYPASS0	Bypass PLL 0	S9	Low (C-1)
BYPASS1	Bypass PLL 1	S11	Low (C-1)
BYPASS2	Bypass PLL 2	S13	Low (C-1)
IGNLOCK	Ignore PLL Lock status	S15	High (C-3)

Table 5: GR740 Bootstrap Settings

Signal	Function	Switch	Default
GPIO0	EDCL LINK MACADDR Bit 0	S1	Low (C-1)
GPIO1	EDCL LINK MACADDR Bit 1	S2	High (C-3)
GPIO2	EDCL LINK0 MACADDR Bit 2	S3	High (C-3)
GPIO3	EDCL LINK0 MACADDR Bit 3	S4	Low (C-1)
GPIO4	EDCL LINK1 MACADDR Bit 2	S6	High (C-3)
GPIO5	EDCL LINK1 MACADDR Bit 3	S8	Low (C-1)
GPIO6	SPW ROUTER INT MODE 0	S10	Low (C-1)
GPIO7	SPW ROUTER INT MODE 1	S12	Low (C-1)
GPIO8	EDCL LINK0 TRAFFIC	S14	High (C-3)
GPIO9	EDCL LINK1 TRAFFIC	S16	High (C-3)
GPIO10	PROM WIDTH	S17	Low (C-1)
GPIO11	SPW CLOCK GATE	S18	Low (C-1)
GPIO12	SPW ROUTER ID BIT 0	S19	Low (C-1)
GPIO13	SPW ROUTER ID BIT 1	S20	Low (C-1)
GPIO14	PROM EDAC	S21	Low (C-1)
GPIO15	PROM/IO	S22	High (C-3)

Table 6: GR740 GPIO Bootstrap Settings

5.1.3 Other configurable switches default settings

Signal	Function	Switch	Default
GPIO2_12	To select FPIO6 or BPIO5	S23	FPIO6 High (C-3)
GPIO2_13	To select FPIO7 or BPIO6	S24	FPIO7 High (C-3)
BPIO 0 to 5	See Table 4 Functions assigned to GPIO2 signals of GR740	S26 to S41	Float (C-1)

Table 7: Other configurable switches default settings

5.2 Jumper configurations

The default status of the Jumpers on the boards is as shown in Table 8. (Other configurations may be defined by the user).

5.2.1 Default Setting of Jumpers – GR-VPX-GR740

Jumper	Default Jumper Setting	Comment
JP1	Installed	Remove jumper to disable writing to MRAM.
JP2	Not installed	Install to write protect serial SPI Prom
JP3	Connected to Front-Panel 1-2 3-4	Connects front panel RESET and BREAK push button to JP3
JP4	-	-
JP5	Not installed	VC0-PROG, do not install for parameters to be loaded via I2C
JP6	Installed	VC0-CLKSEL; MEM_CLK_P and N generates SDCLK's
JP7	Not installed	Install jumper for Watchdog signal to trigger reset
JP8	1-2 3-4 5-6 7-8	Connects ASIC JTAG to FTDI chip
JP9	1-2 3-4 5-6 7-8	GR740 UART 0 and 1 connects to FTDI chip
JP10	1-2	An SMB connector is available on the front panel for PPS input. This signal is terminated with a 50 Ohm load and buffered. The buffered signal is connected to the *JP10 Jumper input (1)* and, via the mezzanine connector. This jumper when configured as 1-2 the PPS from the external input is passed to *GR740 processor* and also to the backplane (as a differential signal on the AUXCLK_OUT pins). This jumper when configured as 2-3 the PPS from the external input is passed to mezzanine connector and the output from the mezzanine connector (PPS_OUT) is connected with the *GR740 processor* and also to the backplane (as a differential signal on the AUXCLK_OUT pins). This setting allows the PPS to be processed by the Mezzanine board if such implementation is required for the user.
JP11	1-2	An onboard oscillator generates a 25 MHz clock. This signal is connected to the *JP11 Jumper input (1)* and, via the mezzanine connector to the mezzanine connector. This jumper when configured as 1-2 the clock is passed to the backplane (as a differential signal on the REF_CLK_P and N pins). This jumper when configured as 2-3 the clock is passed to mezzanine connector and the output from the mezzanine is connected to the backplane (as a differential signal on the REF_CLK_P and N pins).
JP12	Installed	Option to provide 3V3 from Main Board to Mezzanine
JP13	Not installed	Configuration options for Versaclock PLL ranges
JP14	Not installed	VC1-PROG, do not install for parameters to be loaded via I2C
JP15	Installed	VC1-CLKSEL; XTAL generates 25MHZ clock

Table 8: Default Setting of Jumpers – GR-VPX-GR740

6 Interfaces and Configuration

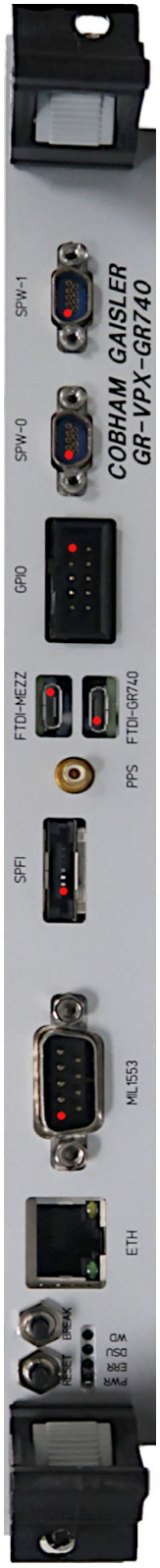

Figure 6-1: Front Panel View (pins 1 marked red)

Note in Figure 6-1 the SpW and SpFI are from the mezzanine board which are not part of the GR-VPX-GR740 base board.

6.1 List of Connectors – GR-VPX-GR740

Name	Function	Type	Description
J1	POWER_IN	MOLEX_6410_2pin	DC power input connector (only to be used in Stand-alone usage)
J2	MIL1553	D9-Male	MIL-1553 dual interface
J3	ETH	RJ45	GB Ethernet Connector
J4	PPS	SMB	Pulse-Per-Second Input
J5	FPIO	10 pin 0.1” Header	Front panel Input/Output
J6	SODIMM	144 pin SODIMM conn.	SDRAM interface
J7	JTAG-GR740	6 pin 0.1” header	GR740 JTAG interface
J8	FTDI-Serial	Micro-USB	FTDI USB to serial interface – JTAG & UART
J9	Mezzanine	FMC-HPC-400 pin	Mezzanine interface
J10	SPW-HDR	MDM_9S	SpaceWire interface
J11	FPGA-program	5x2 pin 0.1” Header	Programming header for FPGA
P0	VPX Backplane	TE 1410189-3, Plug	VPX Backplane Connector VITA46, 56 pos.
P1	VPX Backplane	TE 1410187-3, Plug	VPX Backplane Connector VITA46, 112 pos.
P2	VPX Backplane	TE 1410187-3, Plug	VPX Backplane Connector VITA46, 112 pos
P3	VPX Backplane	TE 1410187-3, Plug	VPX Backplane Connector VITA46, 112 pos
P4	VPX Backplane	Not fitted	
P5	VPX Backplane	TE 1410187-3, Plug	VPX Backplane Connector VITA46, 112 pos
P6	VPX Backplane	Not fitted	

Table 9: List of Connectors – GR-VPX-GR740

6.2 List of Connectors – GR-VPX-SPW-MEZZ

Name	Function	Type	Description
J8	SPW-1	MDM_9S	SpaceWire interface GR740 ROUTER PORT 2
J9	SPW-0	MDM_9S	SpaceWire interface GR740 ROUTER PORT 1

Table 10: List of Connectors – GR-VPX-SPW-MEZZ

Pin	Name	Comment
1	**DGND**	Ground
2	+VIN	Power Input +5V to +12V, typically TBD A

Table 11: J1 POWER – External Power Connector

Pin	Name	Comment
1	BUS_0	BUS_0 positive
6	GND	Ground
2	BUS_0B	BUS_0 negative
7		No connect
3		No connect
8		No connect
4	BUS_1	BUS_1 positive
9	GND	Ground
5	BUS_1B	BUS_1 negative

Table 12: J2 Dual MIL-STD-1553 interface connections

Pin	Name	Comment
1	TPFOP	Output +ve
2	TPFON	Output -ve
3	TPFIP	Input +ve
4	TPFOC	Output centre-tap
5		No connect
6	TPFIN	Input -ve
7	TPFIC	Input centre-tap
8		No connect

Table 13: J3 RJ45-ETHERNET Connector

Pin	Name	Comment
INNER	+IN	Inner Pin, Pulse Per Second,+3V3 logic
OUTER	**DGND**	Outer Pin Return

Table 14: J4 PPS Input

FUNCTION	CONNECTOR PIN			FUNCTION
FPIO0	1	■	2	FPIO1
FPIO2	3	□	4	FPIO3
FPIO4	5	□	6	FPIO5
FPIO6	7	□	8	FPIO7
Opt. +3V3	9	□	10	DGND

Table 15: J5: Front Panel Input/Output pins

FUNCTION	ASIC PIN	CONNECTOR PIN		ASIC PIN	FUNCTION
DGND		1	2		DGND
DQ0		3	4		DQ24
DQ1		5	6		DQ25
DQ2		7	8		DQ26
DQ3		9	10		DQ27
+3.3V		11	12		+3.3V
DQ4		13	14		DQ28
DQ5		15	16		DQ29
DQ6		17	18		DQ30
DQ7		19	20		DQ31
DGND		21	22		DGND
SDDQM0		23	24		SDDQM2
SDDQM1		25	26		SDDQM4
+3.3V		27	28		+3.3V
A2		29	30		A5
A3		31	32		A6
A4		33	34		A7
DGND		35	36		DGND
DQ8		37	38		DQ32
DQ9		39	40		DQ33
DQ10		41	42		DQ34
DQ11		43	44		DQ35
+3.3V		45	46		+3.3V
DQ12		47	48		DQ36
DQ13		49	50		DQ37
DQ14		51	52		DQ38
DQ15		53	54		DQ39
DGND		55	56		DGND
nc		57	58		nc
nc		59	60		nc
SDCLK0		61	62		SDCKE0
+3.3V		63	64		+3.3V
SDRASN		65	66		SDCASN
SDWEN		67	68		SDCKE1
SDCSN0		69	70		A17
SDCSN1		71	72		A14
nc		73	74		SDCLK1
DGND		75	76		DGND
nc		77	78		nc
nc		79	80		nc
+3.3V		81	82		+3.3V
DQ16		83	84		DQ40
DQ17		85	86		DQ41
DQ18		87	88		DQ42
DQ19		89	90		DQ43
DGND		91	92		DGND
DQ20		93	94		DQ44
DQ21		95	96		DQ45
DQ22		97	98		DQ46
DQ23		99	100		DQ47
+3.3V		101	102		+3.3V
A8		103	104		A9
A10		105	106		A15 (SBA0)
DGND		107	108		DGND
A11		109	110		A16 (SBA1)
A12		111	112		A13
+3.3V		113	114		+3.3V
SDDQM2		115	116		SDDQM5
pulled high		117	118		pulled high
DGND		119	120		DGND
nc		121	122		nc
nc		123	124		nc
nc		125	126		nc
nc		127	128		nc
+3.3V		129	130		+3.3V
nc		131	132		nc
nc		133	134		nc
nc		135	136		nc
nc		137	138		nc
DGND		139	140		DGND
SDSDA / pulled high		141	142		SDSCL / pulled high
+3.3V		143	144		+3.3V

Table 16: J6: SDRAM SODIMM socket Pin-out

Pin	Name	Comment
1	VJTAG	3.3V
2	**DGND**	Ground
3	TCK	JTAG: TCK
4	TDO	JTAG: TDO
5	TDI	JTAG: TDI
6	TMS	JTAG: TMS

Table 17: J7 GR740 – JTAG Connector

Pin	Name	Comment
1	VBUS	+5V (from external host)
2	DM	Data Minus
3	DP	Data Plus
4	ID	Not used
5	**DGND**	Ground

Table 18: J8 USB Micro connector – FTDI Quad Serial Link

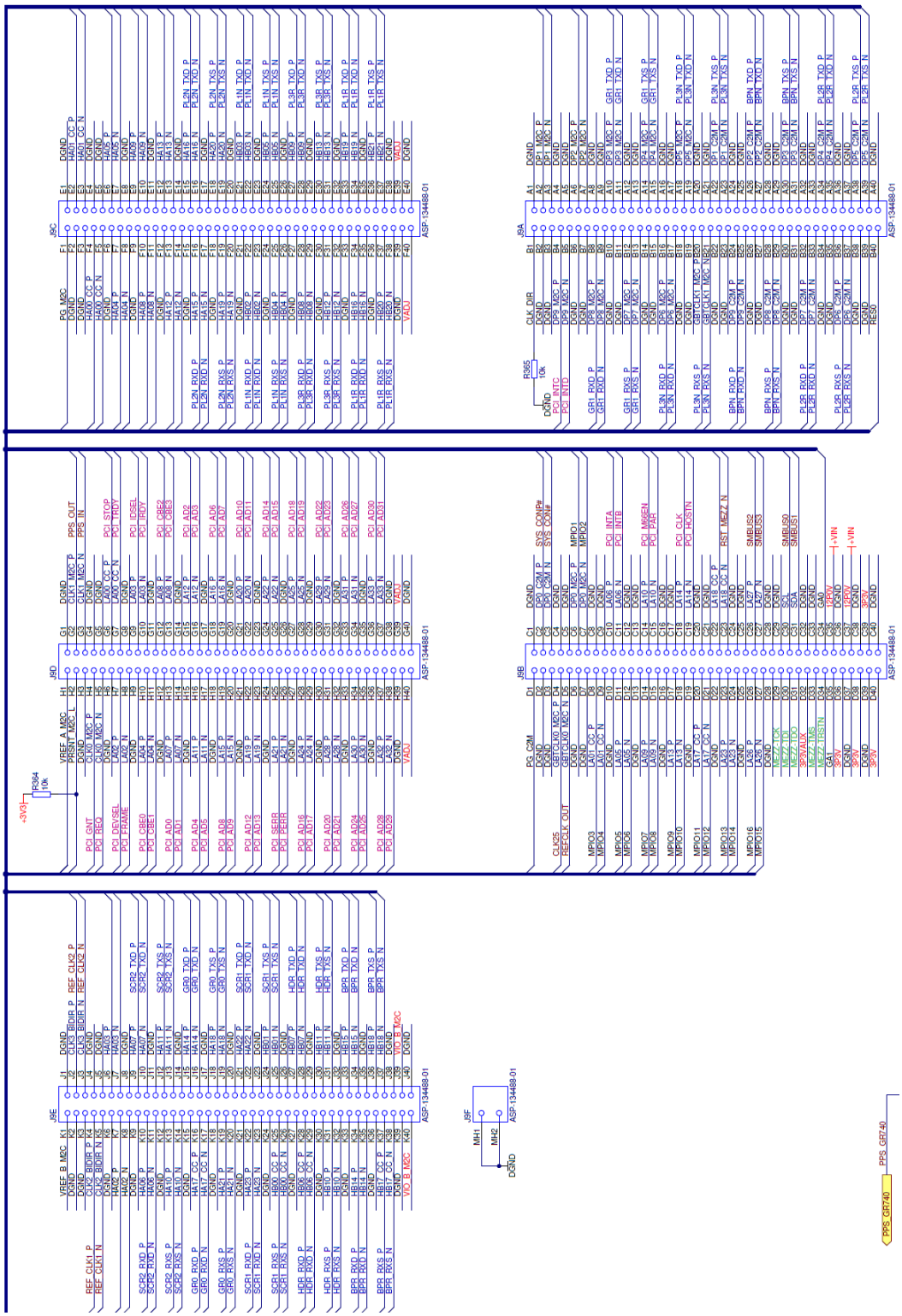

Table 19: J9 Mezzanine Connector – Female

Pin	Name	Comment
1	DIN0+	Data In +ve
6	DIN0-	Data In -ve
2	SIN0+	Strobe In +ve
7	SIN0-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT0+	Strobe Out +ve
4	SOUT0-	Strobe Out -ve
9	DOUT0+	Data Out +ve
5	DOUT0-	Data Out -ve

Table 20: J10 SPW-HDR interface connections

Pin	Name	Comment
1	F-TCK	JTAG: TCK
2	DGND	Ground
3	F-TDO	JTAG: TDO
4	nc	no connect
5	F-TMS	JTAG: TMS
6	VREF	3.3V
7	VPUMP	Programming Voltage
8	F-TRSTN	JTAG: TRSTN
9	F-TDI	JTAG: TDI
10	**DGND**	Ground

Table 21: J11 FPGA– JTAG Connector

6.3 List of Oscillators, Switches and LED's - GR-VPX-GR740

Name	Function	Description
X1	MAIN-OSC	50 MHz (soldered) for SYS-CLK, SPW-CLK, MEM-CLK, FPGA-CLK
X2	MIL1553-CLK	20 MHz oscillator (soldered)
X3	CLK25	25 MHz oscillator (soldered) to Mezzanine connector
Y1	XTAL-25MHz	25 MHz crystal (soldered) for Ethernet PHY
Y2	XTAL-12MHz	12 MHz crystal (soldered) for FTDI interface
Y3	XTAL-25MHz	25 MHz crystal (soldered) for Clock generator

Table 22: List and definition of Oscillators and Crystals

Name	Function	Description
D2	POWER	3.3V power good
D3	ERR	GR740 ERRORN
D4	WD	GR740 Watchdog
D5	DSUACT	GR740 DSU Active
D7	PLLLOCK0	GR740 PLL lock status 0
D8	PLLLOCK1	GR740 PLL lock status 1
D9	PLLLOCK2	GR740 PLL lock status 2
D10	PLLLOCK3	GR740 PLL lock status 3
D11	PLLLOCK4	GR740 PLL lock status 4
D12	PLLLOCK5	GR740 PLL lock status 5
D13	FP0	FPGA Status

Table 23: List and definition of PCB mounted LED's

Name	Function	Description
S1-S4, S6, S8, S10, S12, S14, S16-S22	GPIO0-15	SP3T – sets GPIO[0-15] to pull-up, float, pull-down
S5	DSU Enable	SP3T – sets DSUEN to pull-up, float, pull-down
S7	MEM-CLKSEL	SP3T – sets MEM-CLKSEL to pull-up, float, pull-down
S9	BYPASS0	SP3T – sets PLL BYPASS0 to pull-up, float, pull-down
S11	BYPASS1	SP3T – sets PLL BYPASS1 to pull-up, float, pull-down
S13	BYPASS2	SP3T – sets PLL BYPASS2 to pull-up, float, pull-down

Name	Function	Description
S15	IGNLOCK	SP3T – sets IGLOCK to pull-up, float, pull-down
S23	GPIO2_12	SP3T selects – GPIO2_12 source
S24	GPIO2_13	SP3T selects – GPIO2_13 source
S25	RESET	Push Button Reset
S26-S33	BP0-BP5	SP3T selects Backpanel IO signals – active when BP6 = ‘0’
S34-S41	BP0-BP5	SP3T selects Backpanel IO signals – active when BP6 = ‘1’

Table 24: List and definition of Switches

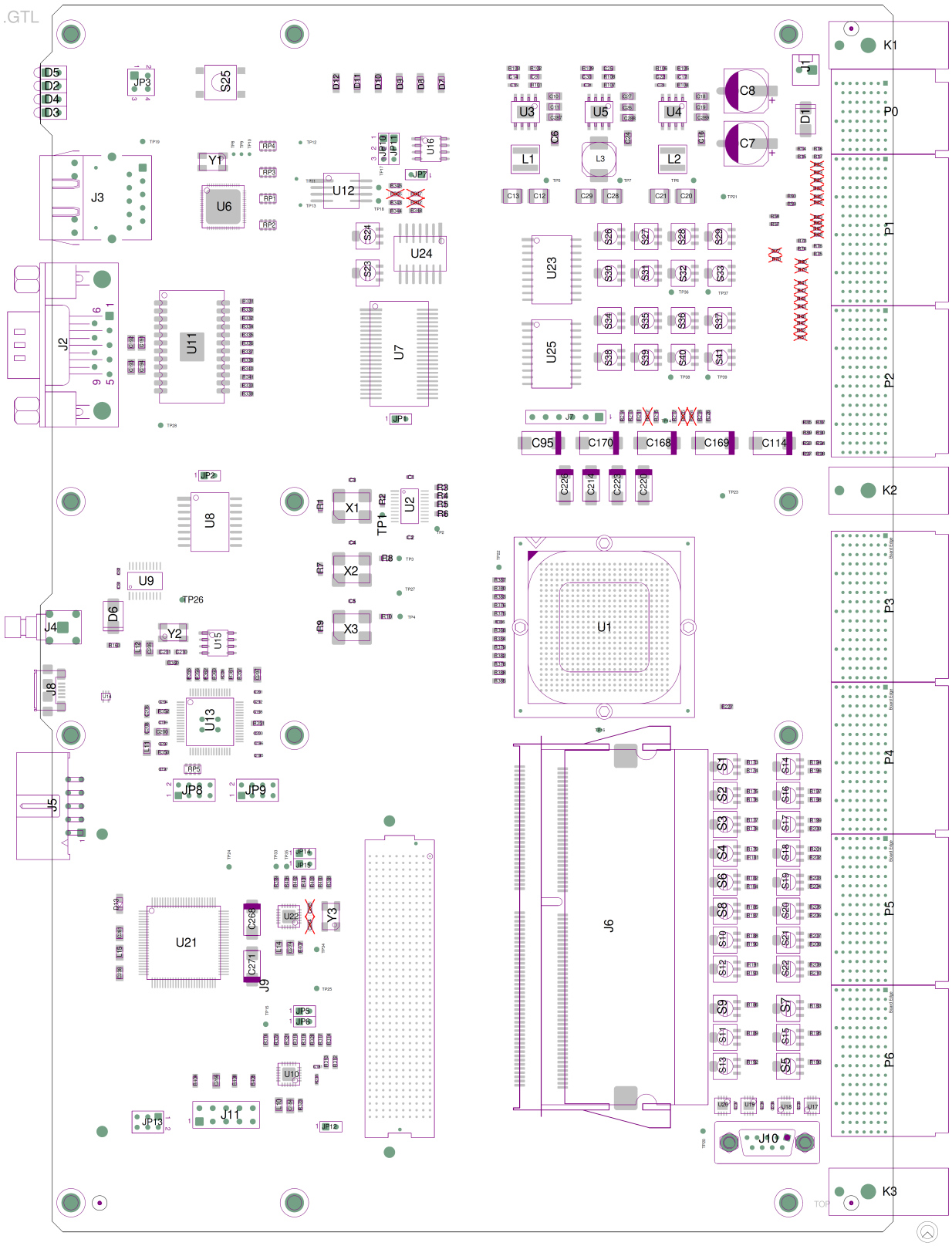

Figure 6-2: GR-VPX-GR740 PCB Top View
(extract from [RD4]

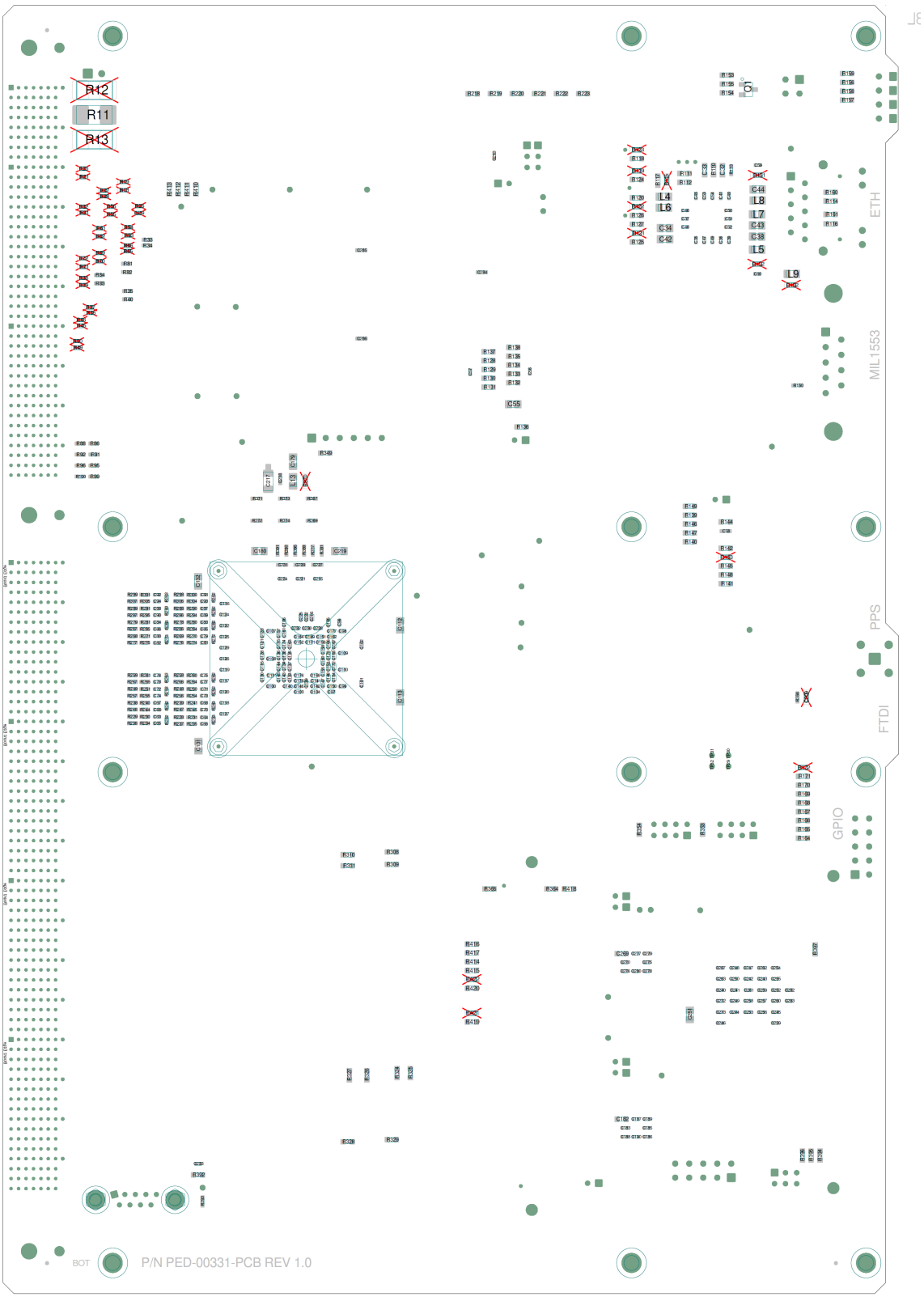

Figure 6-3: GR-VPX-GR740 PCB Bottom View (extract from [RD4]

7 Change Record

Issue	Date	Section / Page	Description
0.0	-	All	Draft Issue
1.0	2019-09-17	Default Jumper values and Switch settings.	First Issue
1.1	2020-04-29	Updated section 4.7 GPIO section with more information.	Second issue with updated details
1.2	2020-08-18	Major change	Removed the Mezzanine board details since it is not part of the delivered GR-VPX-GR740 board product.
1.3	2020-10-09	Fixed Minor typos	The mezzanine connector on board is of type Female. PCI_HOSTN is pulled High on board the GR-VPX-GR740.
1.4	2020-11-06	Section 4.7, 4.8 and 5.1.1 Section 4.1 Table 8	The DSUEN switch named correctly as S5 in section 4.8. Clear description of SP3T switches, updated section 4.7 and 5.1.1. Details of the new mezzanine board (GR-VPX-SPW-MEZZ which provides two SpaceWire interfaces in the Front panel) are included. Jumper JP12 installed by default, to to provide 3V3 from Main Board to Mezzanine

Cobham Gaisler AB
Kungsgatan 12
411 19 Göteborg
Sweden
www.cobham.com/gaisler
sales@gaisler.com
T: +46 31 7758650
F: +46 31 421407