GR718B External bias ciruit for floating LVDS input

Application note 2019-07-30

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Issue 0.3

CHANGE RECORD

Issue	Date	Section / Page	Description
0.1	2017-02-03		First draft issue of this application note.
0.2	2017-02-09		Removed all associations to FMECA (failure-mode analysis for flight implementation on PCB). Note that from FMECA point of view, a resistor solution on PCB will not remove the open circuit failure mode, since open circuit in PCB pad or bondwire still exist.
0.3	2019-07-30	Chapter 6	Corrected mathematical calculations

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1 INTRODUCTION

1.1 Scope of the Document

This document establishes the application note for avoiding uncertain output state of the integrated LVDS receiver of the GR718B when the input is connected improperly.

The work has been performed by Cobham Gaisler AB, Göteborg, Sweden.

1.2 Reference Documents

The following documents are referred as they contain relevant information:

[RD1] GR718B Data Sheet and User's Manual

2 ABBREVIATIONS

LVDS	Low-voltage differential signalling
IO	External Input or Output pin
VDDIO	External Supply Voltage for external Inputs and output pins

3 INTRODUCTION

When the GR718B LVDS inputs are left floating or connected improperly an external biasing circuit using discrete resistors can be used to set the internal LVDS receiver to a known state.

An open or floating port will not affect the reliability as along as absolute maximum rating isn't exceeded for the LVDS input.

For more information about the GR718B device see GR718B Data Sheet and User's Manual.

4 FLOATING LVDS INPUT DEFINITION

The LVDS line has three possible states. Two are the active states where the LVDS line driver is either in the logic HIGH state or logic LOW state. The third state is the un-driven state. This could occur if:

1. The LVDS driver is in TRI-STATE
2. The LVDS driver is powered-off (V_{DDIO} = 0V or open)
3. The LVDS driver is disconnected from the line (unplugged)

5 EXTERNAL BIAS CIRCUIT

The bias circuit consists of three resistors connected to externally to the receiver input. The three resistors are used as a voltage divider between V_{DDIO} and IO so that there will be a positive offset on the LVDS input voltage V_{ID}.

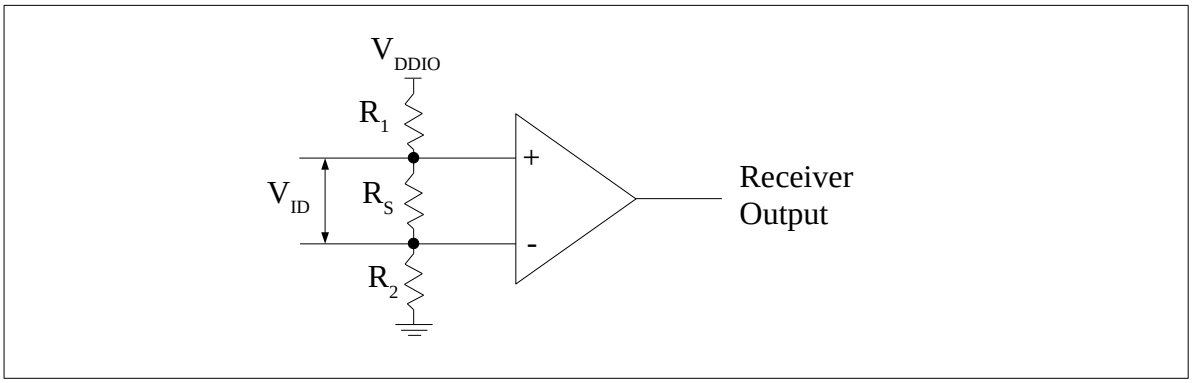

Figure 1 External bias circuit

The resistors R_1 and R_2 sets a positive offset voltage between the two LVDS receiver input pins

when the line is not driven to make sure the driver output is in logic high state. The offset V_{ID} is defined by:

$$V_{ID} = \frac{R_S \times V_{DDIO}}{R_1 + R_2 + R_S}$$

The level of biasing is determined by the noise level in the system and standard values of resistors available.

For example, if a 25 mV bias point is required, first determine the amount of bias current.

$$I_{ID} = \frac{V_{noise}}{R_S} = \frac{25\,mV}{100\,\Omega} = 250\,uA$$

The bias current I_{ID} must be at least an order of magnitude smaller than the 4mA LVDS current.

The total resistance can be determined by the bias supply current from V_{DDIO} to ground

$$R_{ID} = \frac{V_{DDIO}}{I_{ID}} = \frac{3.3\,V}{250\,uA} \approx 13\,k\Omega$$

The LVDS termination resistor RS shall be 100Ω and since its at least an order of magnitude smaller than the total resistance needed it can be ignored.

Next is to determine the ratio between R_2 and R_1:

$$RATIO_{21} = \frac{V_{REFEXT}}{V_{DDIO}} = \frac{1.25\,V}{3.3\,V} = 0.378$$

The $RATIO_{12}$ shall be used to select R_2 and R_1:

$$R_2 = RATIO_{21}\,x\,R_{ID} = 0.378\,x\,13\,k\Omega \approx 5\,k\Omega \rightarrow R_1 = R_{ID} - R_2 \approx 8\,k\Omega$$

This network will provide a bias of approximate +25 mV to the receiver. The R_S resistor should be located as close to the receiver as possible to minimize the stub length. The location of R1 and R2 is less important.

6 EXTERNAL BIAS CIRCUIT FOR UNUSED PORTS

A design may have ports not intended to be used for the application. In such scenario a higher noise margin can be used to minimize the stress on the LVDS input and to reduce the noise inserted into the LVDS receiver.

For ports never to be used by the application the biasing voltage level can be in the range of 200mV to 450 mV to avoid any spurious or erroneous receiver output.

Following the example in chapter 5 gives the resistor values R_1 and R2 according:

$$I_{ID} = \frac{V_{noise}}{R_S} = \frac{450\,mV}{100\,\Omega} = 450\,uA$$

Total resistance:

$$R_{ID} = \frac{V_{DDIO}}{I_{ID}} = \frac{3.3\,V}{450\,uA} \approx 7.3\,k\Omega$$

The $RATIO_{12}$ shall be used to select R_2 and R_1:

$$R_2 = RATIO_{21}\,x\,R_{ID} = 0.378\,x\,7.3\,k\Omega \approx 2.7\,k\Omega \rightarrow R_1 = R_{ID} - R_2 \approx 4.6\,k\Omega$$