GR716-CPCI-DEV
Development Board

FRONTGRADE
Gaisler

USER'S MANUAL

GR716-CPCI-DEV User's Manual

Oct 2023, Version 1.0

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1.1   Scope and Purpose of the Document

This document provides a User's Manual and Interface document for the "GR716-CPCI-DEV" Development and Demonstration board.

The work has been performed by Frontgrade Gaisler AB, Göteborg, Sweden.

1.2   Reference Documents

[RD1]   GR716, Data Sheet and User's Manual",Frontgrade Gaisler, GR716-UM-DS, available from http://www.gaisler.com/index.php/products/components/GR716

[RD2]   GR716-CPCI-DEV_schematic.pdf, Schematic

[RD3]   GR716-CPCI-DEV_assy_drawing.pdf, Assembly Drawing

[RD4]   GRMON3 User's Manual, available from:
         https://www.gaisler.com/index.php/products/debug-tools/grmon3

[RD5]   GR716-BOARD User Manual.pdf, User Manual

2   ABBREVIATIONS

ASIC	Application Specific Integrated Circuit.
DSU	Debug Support Unit
EDAC	Error Detection and Correction
ESA	European Space Agency
ESD	Electro-Static Discharge
ESTEC	European Space Research and Technology Center
GPIO	General Purpose Input / Output
IC	Integrated Circuit
I/O	Input/Output
IP	Intellectual Property
LDO	Low Drop-Out
PCB	Printed Circuit Board
POL	Point of Load
SOC	System On a Chip
SPW	Spacewire
TBC	To Be Confirmed
TBD	To Be Defined

3   INTRODUCTION

3.1   Overview

This document describes the *GR716-CPCI-DEV* Development Board.

Together with the *GR716-DEV* board, this equipment is intended to be used as a platform for the demonstration of the *Frontgrade Gaisler GR716 RAD Hard Microcontroller*.

Furthermore, this board provides developers with a convenient hardware platform for the evaluation and development of software for the *GR716* microcontroller, and allows the *GR716-DEV* board to be installed in a CPCI rack for further integration with other development equipment.

The *GR716* microcontroller features a fault-tolerant LEON3 SPARC V8 processor, communication interfaces and on-chip ADC, DAC, Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support for single 3.3V supply, ideally suited for space and other high-rel applications.
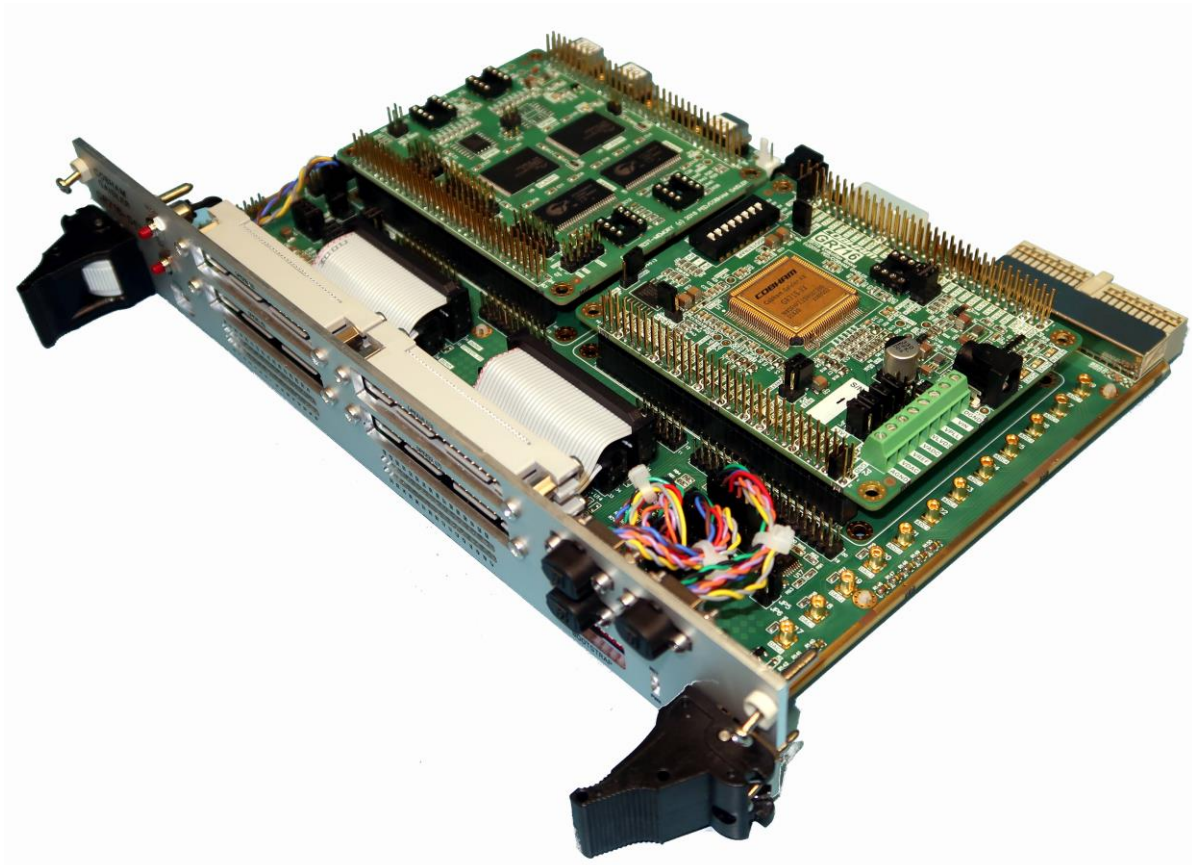
Figure 3-1: GR716-CPCI-DEV Development Board

The board contains the following main items as detailed in section 0 of this document:

- CPCI 6U format (233.35 x 160mm)

- two sites for plug on modules with two 2x32 pin stackable 0.1" headers

- plug on board for configuration of interface routing to peripherals

- connector for single VIN power input (+5V to +12V)

- front panel with

   o 0.1" header connectors for 64 GPIO signals (plus ground)

   o LED's as status indicators for GPIO signals

   o two Spacewire connecotrs (MDM9S)

   o connector for SPI4Space interface (MDM9S)

   o DIP switch for bootstrap settings

   o mini USB connector for FTDI-USB interface

   o LED indicators for Power and ResetOut status

   o RESET_IN and DSUBREAK push button switches

- on-board headers for ribbon cable connection to

   o Packetwire interface

   o CAN interface

   o DSU plus UART interfaces

   o MIL1553 interface

   o SPI peripherals

- miniature coax connectors for 8 x ADC and 4 x DAC analog signals

- jumpers for power supply configuration

- on-board regulators converting from VIN to 3.3V & 1.8V

- sockets for optional on-board oscillator s for

   o SYSCLK

   o SPWCLK

   o MIL1553CLK

   o PWMCLK

3.2   Handling

ATTENTION: OBSERVE PRECAUTIONS FOR

HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an un-powered state.

When operating the board in a 'stand-alone' configuration, the power supply should be current limited to prevent damage to the board or power supply in the event of an over-current situation.

This board is intended for commercial use and evaluation in a standard laboratory environment, nominally, 20°C. All devices are standard commercial types, intended for use over the standard commercial operating temperature range (0 to 70ºC).

4 BOARD DESIGN

4.1 Board Block Diagram

The *GR716-CPCI-DEV* Board provides the electrical functions and interfaces as represented in the block diagram Figure 4-1.
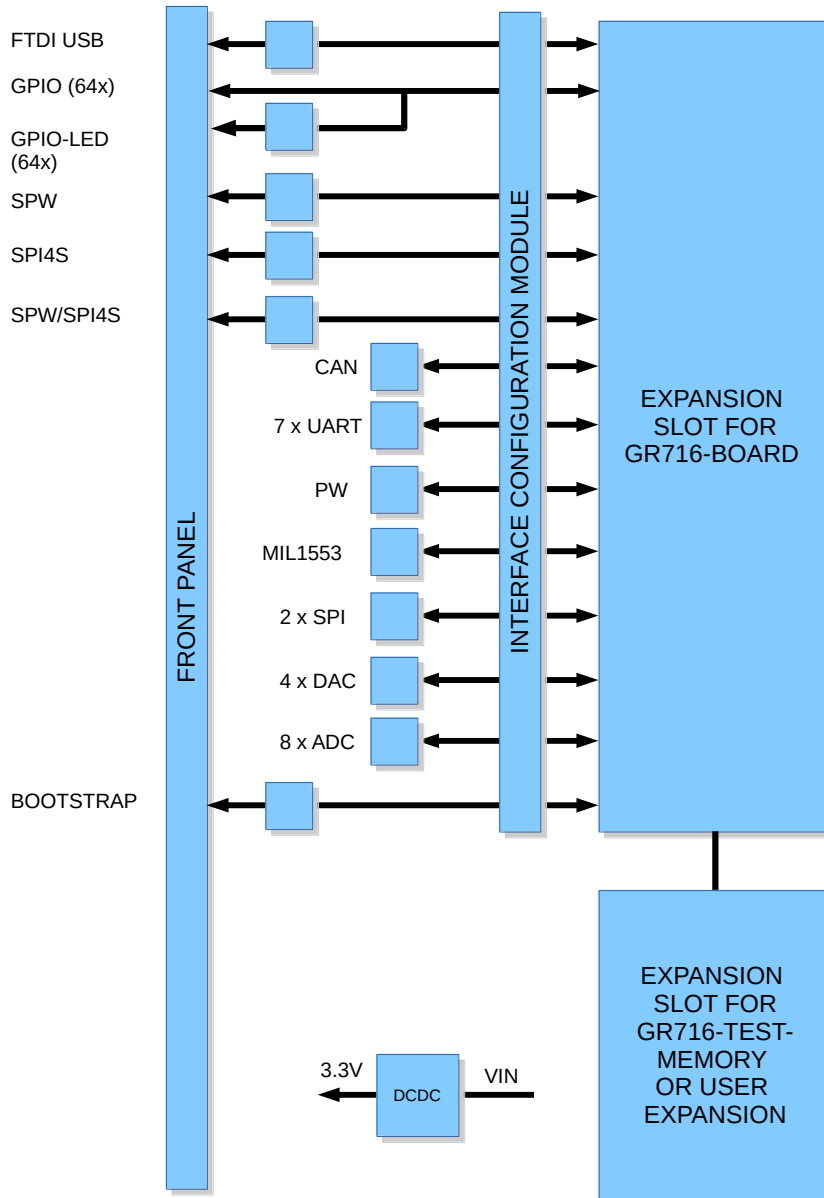
Figure 4-1: GR716-CPCI-DEV Board Block Diagram

Note that not all features and interfaces are simultaneously available since the pins of the *GR716* microcontroller have multiple functions. The available interfaces depends on the configuration and programming of the registers of the *GR716* microcontroller, and on the connections made by the Interface Configuration Module.

4.2 Board Mechanical Configuration

The board (233.35 x 160mm) and can be used 'stand-alone' on the bench-top simply an external +12V power supply connected to connector J32.

A 6U format, 2 slot sized CPCI front panel is fitted to allow the board to be installed in a CPCI rack.
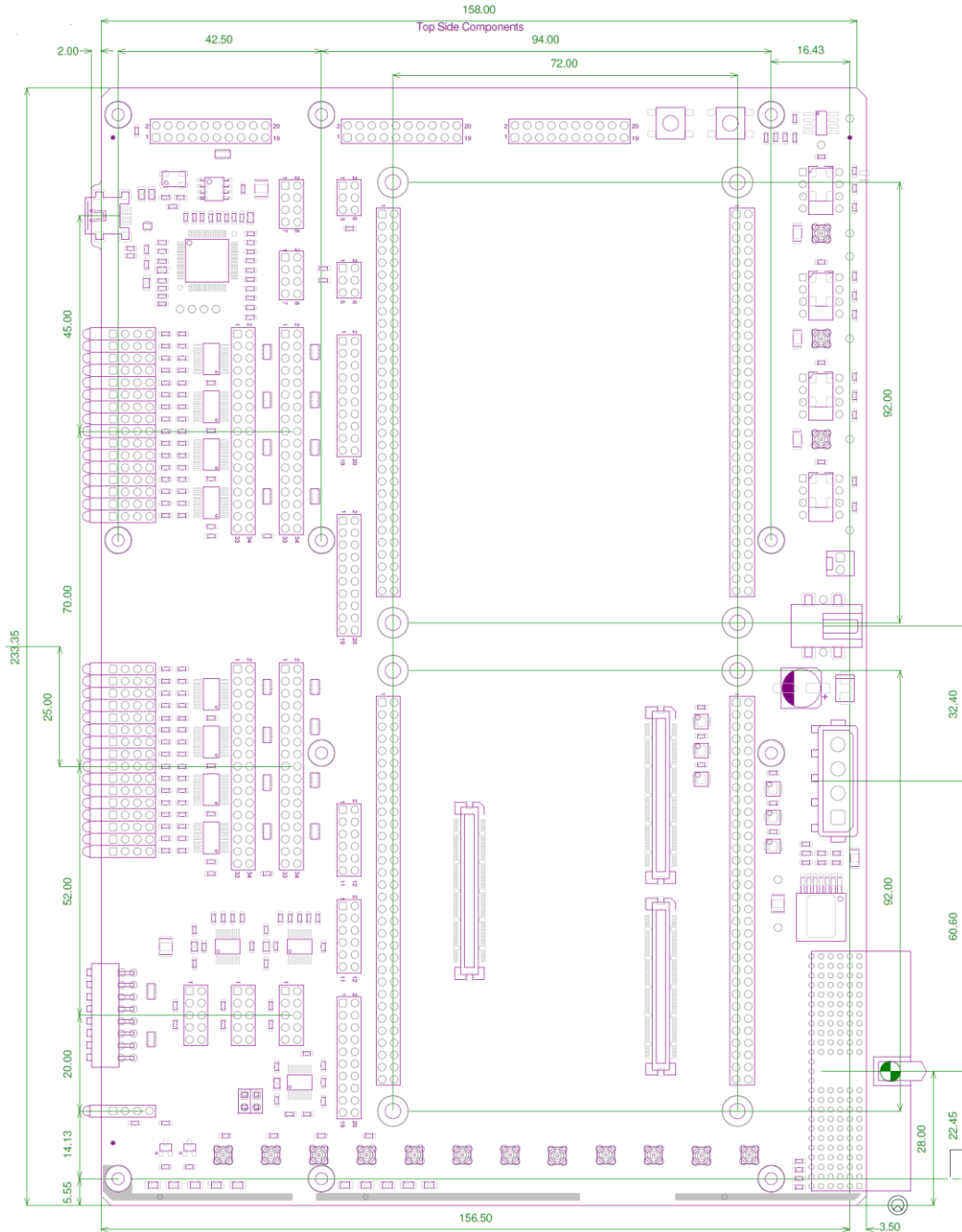
Figure 4-2: GR716-CPCI-DEV Board Dimensions

4.3 GR716-BOARD and Expansion Boards

The *GR716-CPCI-DEV* provides two sites with two 2x32 pin headers to allow the board to function as a carrier board for the *GR716-BOARD (*Figure 4-4*).*

The first set of headers (P1, P2) is intended for mounting the *GR716-BOARD* as shown in Figure 4-3.

The second set of headers connect with a one-to-one correspondence with the first set and is intended for the mounting a *GR716-TEST-MEMORY* board (Figure 4-5), to provide the *GR716-BOARD* with extended FLASH and SRAM external memory.

Alternatively, the second set of headers provides a convenient way for User Defined interface boards to be developed and connected to the *GR716-CPCI-DEV,* if other functions or features are to be demonstrated.
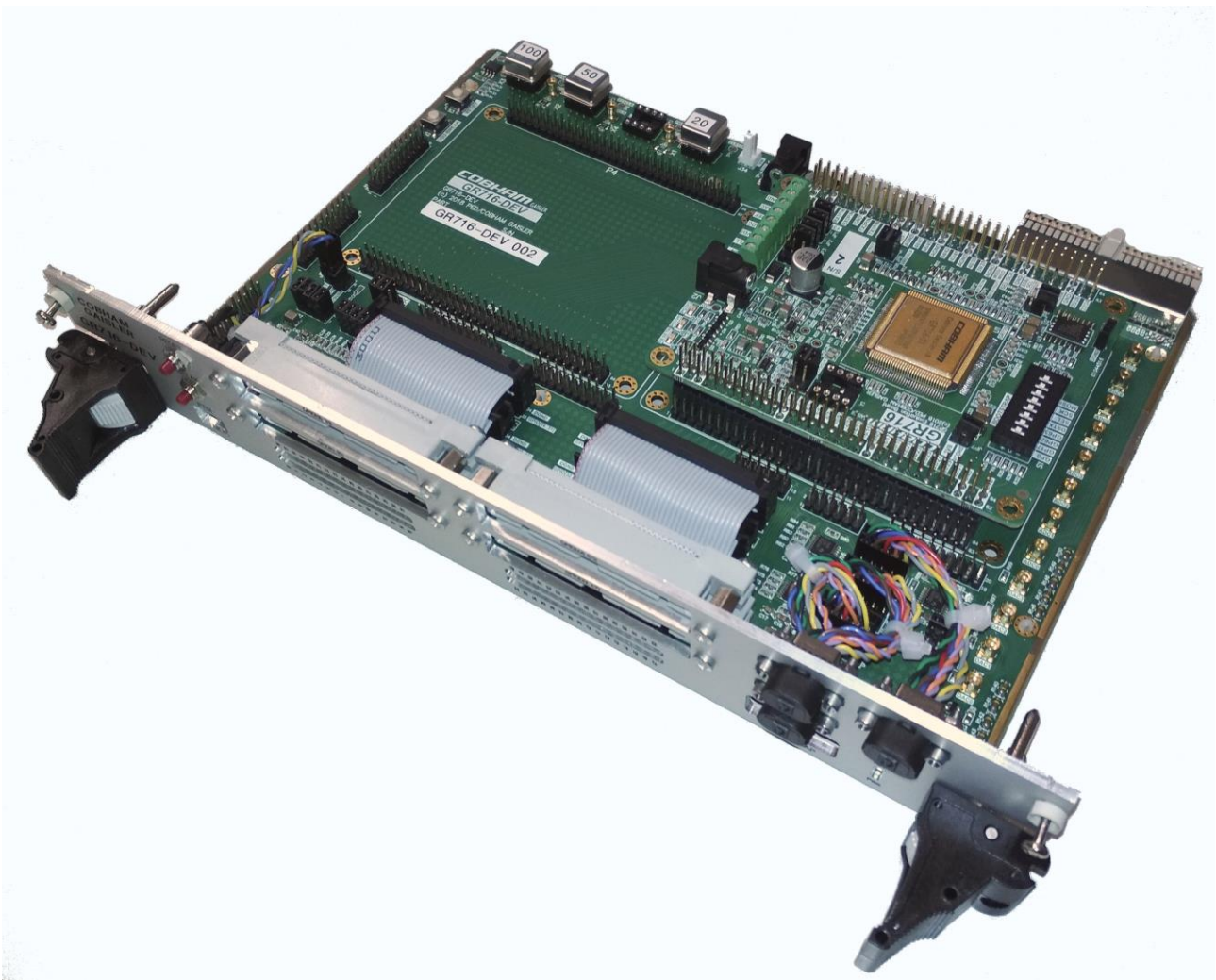
Figure 4-3: GR716-BOARD mounted on a GR716-CPCI-DEV Carrier board
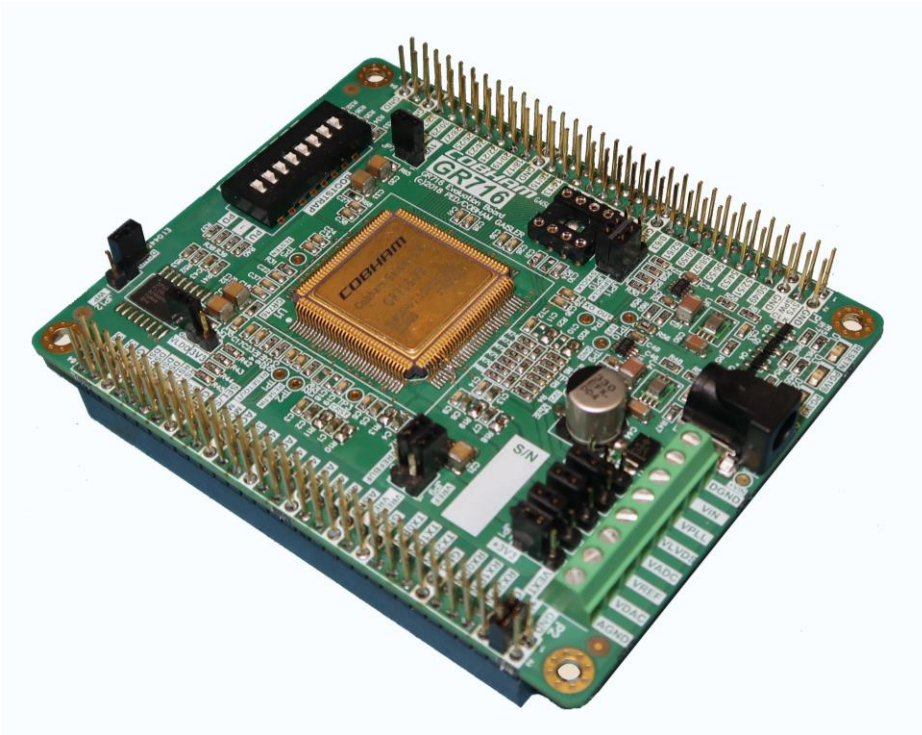
Figure 4-4: GR716-BOARD
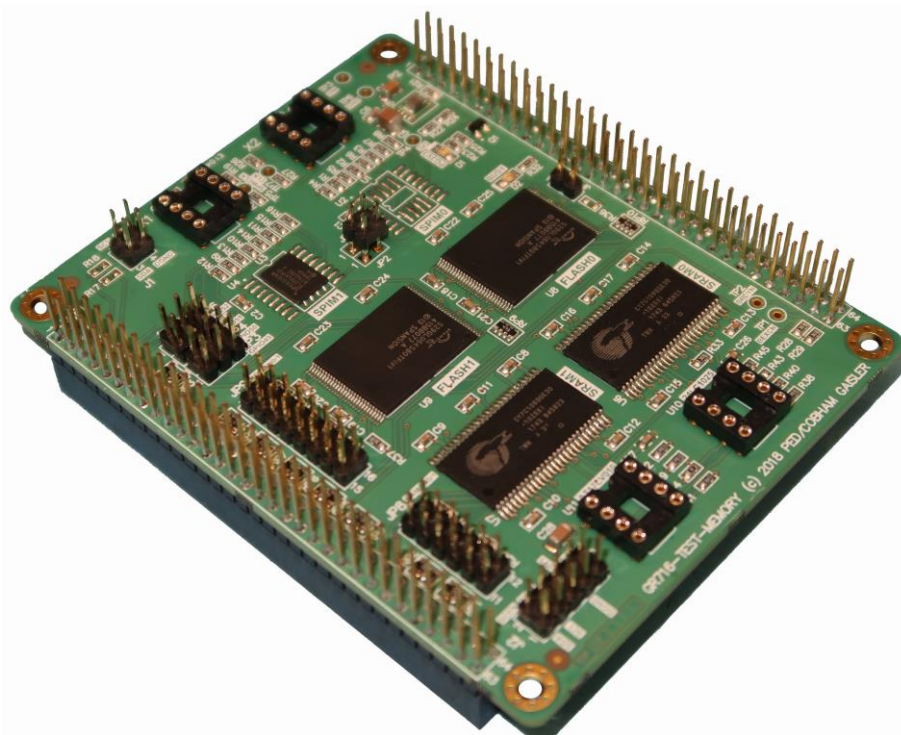
Figure 4-5: GR716-TEST-MEMORY BOARD

4.4   Interface Configuration Board

Since the *GR716* microcontroller has pins with multiple functions, it is necessary to have a way to route pins from the *GR716-BOARD* to the interface circuits in a way that prevents signal and interface conflicts.

This is achieved on the *GR716-CPCI-DEV* board by means of Interface configuration Boards as shown in Figure 4-6.
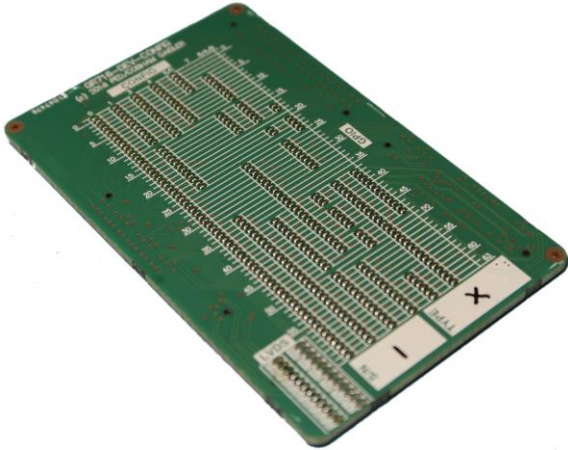
Figure 4-6: Interface Configuration Board

These boards can be configured by means of installing or removing solder bridges in order to route connections from the GPIO pins of the *GR716-BOARD* to the interface circuits on the *GR716-CPCI-BOARD.*

The organisation of the solder bridges corresponds with the organisation of the IO Configuration Options shown in Table 7 of [RD1].

The Interface Configuration Board mounts on to the *GR716-CPCI-DEV board* underneath the Expansion Board, as shown in Figure 4-7.

Figure 4-7: Installed Interface Configuration Board

4.5 GPIO

All 64 GPIO pins can be connected from the *GR716-BOARD* via the Expansion Connector to the *GR716-CPCI-DEV.*

These 64 general Purpose Input Output signals (3.3V LVCMOS voltage levels) are connected to a set of 0.1" pitch pin headers and from there via ribbon cable the front panel of the *GR716-CPCI-DEV* board, thus allowing easy access to these signals, either individually, or with a ribbon cable connection. A series protection resistor of 470 Ohm is included on each signal at the front panel connector.

To indicate the state of the GPIO pins, LED indicators are provided on the front panel.
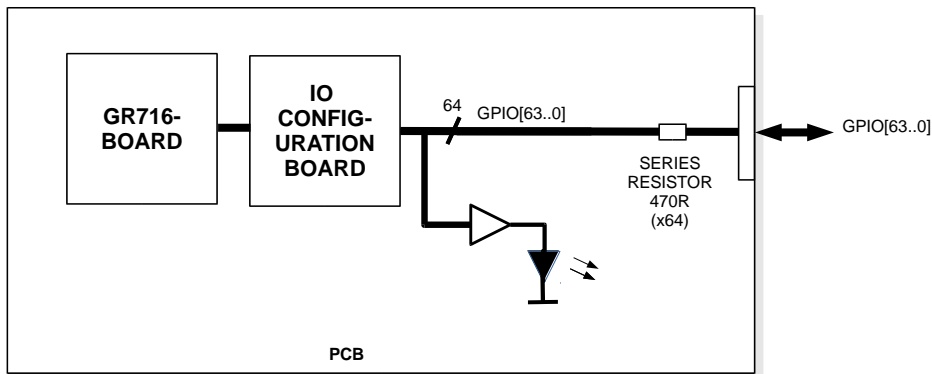
Figure 4-8: GPIO interface

Note that the state of some of the GPIO pins are sampled at power-up or reset of the processor in order to determine initial conditions of a number of internal features, as listed in Table 22 of [RD1] and as described in section 4.15.

4.6 SPW

The *GR-CPCI-DEV* board provides LVDS transceivers to connect the dedicated SpaceWire interface signals of the *GR716* microcontroller to a 10 pin header J7. This header is connected with wire tails to a MDM9S connector on the front panel to provide a standard SpaceWire interface.

4.7 SPI4S

The *GR-CPCI-DEV* board provides LVDS transceivers to connect the dedicated SPI4SPACE interface signals of the *GR716* microcontroller to a 10 pin header J8. This header is connected with wire tails to a MDM9S connector on the front panel.

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4.8 LVDS

The dedicated LVDS interface signals from the *GR716* microcontroller are connected to a 10 pin header J6. Depending on the configuration of the *GR716* microcontroller and Interface Configuration board,, this interface can be used as SpaceWire or as a SPI4SPACE interface.

This header is connected with wire tails to a MDM9S connector on the front panel.
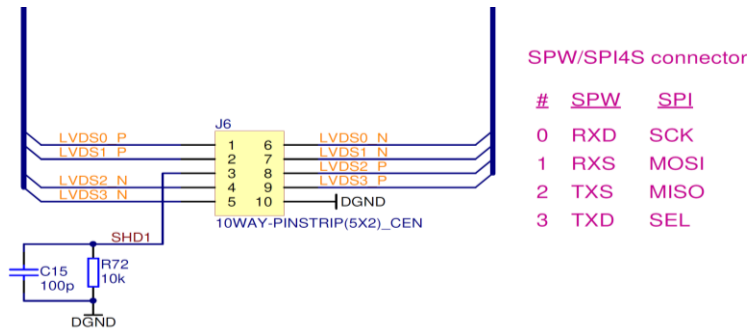
Figure 4-9: Dual purpose LVDS Signal Header

This equipment has SPW ports that use Low Voltage Differential Signalling (LVDS) which has limited common mode voltage protection. To avoid damage to the SPW interfaces due to common mode voltage the following actions should be performed before the equipments that will be connected by SpaceWire are powered on.

- Before connecting any SpaceWire cables, make sure that there is no voltage difference between the different equipment grounds. E.g., measure the voltage between the different equipment grounds with a voltmeter. The result should be close to 0 V.

- After the SpaceWire cables are connected, make sure that the equipment grounds are low ohmic connected to each other. E.g., measure the resistance between the different equipment grounds with a multimeter in resistance mode. The result should be less than 1 Ω.

The SPW standard specification specifies that the cable side outer shield is bonded to the connector shell but does not say anything about the grounding/bonding of the connector side shell. So, you can't be sure that the different equipment grounds are connected only by the SpaceWire cable.

In this equipment the SPW connector side shell is not connected to the local GND of the SPW circuits. The users connecting the board to other equipment only via SPW should ensure grounding via other means (e.g., a dedicated wire).

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4.9   UART-A / UART-B / UART-C

Three 20 pin headers are provided on the *GR716-CPCI-DEV* board to allow various combinations of UART interfaces to be connected with a ribbon cable to a *GR-ACC-6U-UART* accessory board. This can provide up to 6 UART interfaces with RS232 transceivers and standard DSUB-9S connectors

The Headers provide the following combinations of interfaces:

Header J9	Header J10	Header J11	Comment
UART0	UART2	UART4	RX, TX, CTSN, RTSN signals
UART1	UART3	UART5	RX, TX, CTSN, RTSN signals
UART2	UART4	UART0	RX & TX signal
UART3	UART5	UART1	RX & TX signal
UART4	UART0	UART2	RX & TX signal
-	UART1	UART3	RX & TX signal
UART-DSU	-	-	RX & TX signal

Table 1: UART interface Combinations

4.10   CAN

The CAN signals from the *GR716-BOARD* are connected to a header J12.

To provide the necessary CAN transceiver circuits, this header can be connected with a ribbon cable to a *GR-PCI-CAN* accessory board.

4.11   MIL1553

The MIL1553 signals from the *GR716-BOARD* are connected to a header J13.

To provide the necessary MIL-1553 transceiver circuits, this header can be connected with a ribbon cable to a *GR-ACC-GR740* accessory board.

4.12   SPI0 / SPI1

The signals of the SPI0 and SPI1 interfaces from the *GR716-BOARD* are connected to a header J14 & J15 respectively.

This header can be connected with a custom cable to a *GR-ACC-GR740* accessory board.

4.13   PACKETWIRE

The signals of the SPI0 and SPI1 interfaces from the *GR716-BOARD* are connected to a header J16.

This header can be connected with a custom cable to a *GR-TMTC-PW* accessory board.

Note though that the *GR-TMTC-PW* does not accommodate the TX_READY and RX_READY signals.

4.14   DAC0-3 & ADC0-7

The four DAC current outputs from the *GR716-BOARD* are connected to a miniature MMCX coaxial connectors J17 to J20.

The eight ADC voltage inputs to the *GR716-BOARD* are connected to a miniature MMCX coaxial connectors J21 to J27 and J29.

4.15   Bootstrap Signals

A number of features of the *GR716* microcontroller are required to be set at power-on of the processor, by means of bootstrap pins. A number of GPIO and function pins are pre-defined for this purpose, according the definition Table 22 of [RD1].

To define the desired setting, an 8 pole, DIP switch (S1), is provided on the front panel of the *GR716-CPCI-DEV* board to connect these signals to DGND or via pull-up to 3V3.

Note: A DIP switch for setting these Bootstrap signals also exists on the *GR716-BOARD* ([RD5]). The DIP switches on the *GR716-BOARD* should be set to 'float' to ensure that there is no conflict with the DIP switch settings on the front panel of the *GR716-CPCI-DEV* board.

Pin	Function	Open	Closed	Default
GPIO0	Disable EDAC	'1'	'0'	'1'
GPIO17	Bypass Internal Boot Prom	'1'	'0'	'0'
GPIO62	Enable Memory Test	'1'	'0'	'0'
GPIO63	Redundant Memory Available	'1'	'0'	'0'
DSUTX	Copy ASW image/SPW default frequency	'1'	'0'	'0'
SPIM_MOSI	Remote Access/Boot from Memory	'1'	'0'	'0'
SPIM_SCK	Boot Source 0	'1'	'0'	'0'
SPIM-SEL	Boot Source 1	'1'	'0'	'0'

Table 2: Bootstrap Resistor Settings

4.16 Debug Support Unit Interfaces

Program download and debugging to the processor is performed using the GRMON Debug Monitor tool from Frontgrade Gaisler ([RD4]). The *GR716* microcontroller provides a UART based DSU interface for Debug and control of the processor by means of a host terminal, as represented in Figure 4-10.

Four control signals from the Debug Support Unit interface to the processor are implemented:

DSUTX   Debug UART Transmit

DSURX   Debug UART Receive

DSUEN   This signal is pulled high on the board to enable Debugging

DSUBRE   This signal is pulled low on the board

These signals are connected via the Expansion Connector interface from the *GR716-BOARD* to an FTDI USB interface. This allows a USB connection to be made to a host computer.
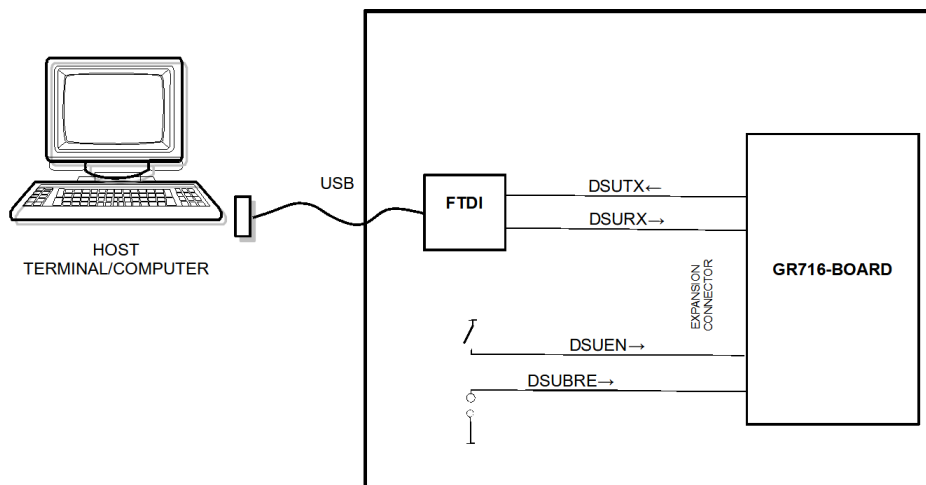
Figure 4-10: Debug Support Unit connections

4.17 Oscillators and Clock Inputs

The *GR716-CPCI-DEV* Board provides four DIL sockets to allow an external oscillator clocks to be connected to the following clock inputs of the *GR716* microcontroller:

> EXT_SYSCLK
>
> EXT_SPWCLK
>
> EXT_1553_CLK
>
> EXT_PWMCLK

For more details of the internal Crystal Oscillator, PLL structure and clock gating features of the *GR716*, please refer to sections 9 and 10 of [RD1].

4.18 Power Supply and Voltage Regulation

The power configuration is represented in Figure 4-11.

The main voltage supply input can be provided from one of the following sources:

1. VIN input supply via connector J33.
2. VIN input supply via connector J34.
3. VIN provided via CPCI Backplane connector.

VIN is regulated on the *GR716-CPCI-DEV* board to with a local Point-of-Load DC/DC converter to generate a +3V3 voltage supply for the local circuits on the *GR716-CPCI-DEV* board.

VIN is also connected to the *GR716-BOARD* via the expansion connector P2, where it is further regulated for the *GR716* microcontroller, as described in [RD5].

The VIN voltage should have a nominal value of 12V. However, due to the wide input voltage range capability of the POL DC/DC converters used, the input voltage may range from 5V to 17V.

Note though that, due to the 15V transzorb protection diode on the *GR716-CPCI-DEV* board, the input voltage on this board should not exceed 14.5V.
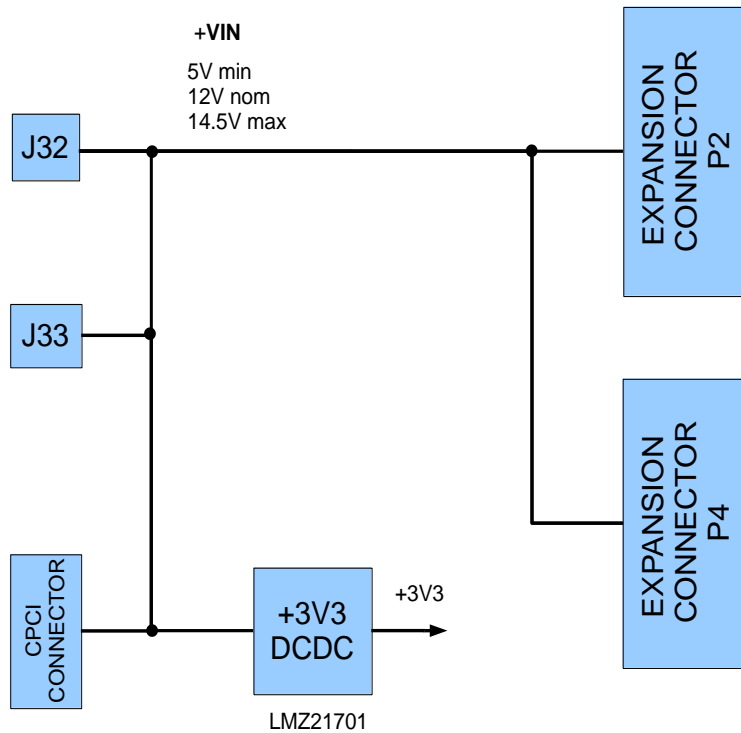
Figure 4-11: Power Regulation Scheme

4.19 Reset Circuit and Button

The *GR716* microcontroller includes an internal RESET circuit with Brown-out detector to reset the processor and its peripherals (see section 8 of [RD1]).

The resulting low reset signal is present on the microcontroller pin *RESET_OUT_N*. This signal is connected to the expansion connector, P2.

A manual reset of the microcontroller can be generated using the *RESET_IN_N* signal. This signal is present on the expansion connector P2, and can be driven from an external circuity if required. A miniature push button switch is provided on the front panel of the *GR716-CPCI-DEV* board to pull this signal low, when the button is pressed.

5   SETTING UP AND USING THE BOARD

The board is provided with a default configuration set by bootstrap settings.

For additional information, refer to [RD2] and for information about the Bootstrap signals, refer to section 4.15.

To operate the board stand alone on the bench top, install the power configuration jumpers appropriately, and +12V supply to the board connector J32.

ATTENTION! To prevent damage to board, please ensure that the correct power supply voltage and polarity is used with the board.

Do not exceed +14.5V at the power supply input, as this may damage the board.

The POWER_3V3 power good LED on the front panel should be illuminated indicating that the power supply is present and the board is generating the supply voltages that it requires.

Upon power on, the Processor will start executing instructions beginning at the memory location 0x02000000, which is the start of the external SPI Flash. If the SPI Flash is 'empty' or no valid program is installed, the first executed instruction will be invalid, and the processor will halt with an ERROR condition.

To perform program download and software debugging on the hardware it is necessary to use the Frontgrade Gaisler GRMON3 debugging software, installed on a host PC (as represented in Figure 4-10). Please refer to the GRMON3 documentation for the installation of the software on the host PC (Linux or Windows), and for the installation of the associated hardware dongle.

To perform software download and debugging on the processor, a link from the Host computer to the DSU interface of the board is necessary. As described in section 4.16 this is achieved via the FTDI USB interface.

Program download and debugging can be performed in the usual manner with GRMON3. More information on the usage, commands and debugging features of GRMON3, is given in the GRMON3 Users Manuals and associated documentation,[RD4].

6 INTERFACES AND CONFIGURATION

6.1 List of Connectors

Name	Function	Type	Description
PI	EXPANSION-1	2x32 pin 0.1" Header	Expansion connector-1
P2	EXPANSION-2	2x32 pin 0.1" Header	Expansion connector-2
P3	EXPANSION-1	2x32 pin 0.1" Header	Expansion connector-3
P4	EXPANSION-2	2x32 pin 0.1" Header	Expansion connector-4
J1	FTDI-USB	Mini USB	FTDI Serial to USB interface
J2	GPIO[15..0]	2x17 pin 0.1" Header	GPIO signals 0-15
J3	GPIO[31..16]	2x17 pin 0.1" Header	GPIO signals 16-31
J4	GPIO[47..32]	2x17 pin 0.1" Header	GPIO signals 32-47
J5	GPIO[63..48]	2x17 pin 0.1" Header	GPIO signals 48-63
J6	SPW0	2x5 pin 0.1" Header	Connects to front panel MDM9S connector
J7	SPW1	2x5 pin 0.1" Header	Connects to front panel MDM9S connector
J8	SPI4S	2x5 pin 0.1" Header	Connects to front panel MDM9S connector
J9	UART-A	2x10 pin 0.1" Header	
J10	UART-B	2x10 pin 0.1" Header	
J11	UART-C	2x10 pin 0.1" Header	
J12	CAN	2x10 pin 0.1" Header	
J13	MIL1553	2x10 pin 0.1" Header	
J14	SPI0	2x6 pin 0.1" Header	
J15	SPI1	2x6 pin 0.1" Header	
J16	PACKETWIRE	2x10 pin 0.1" Header	Interface signals for Packetwire interface
J17-J20	DAC0-3	MMCX	
J21-J27	ADC0-6	MMCX	
J28	EXT_SYSCLK	MMCX	
J29	ADC0-7	MMCX	
J30	EXT_SPWCLK	MMCX	
J31	EXT_PWMCLK	MMCX	

Name	Function	Type	Description
J32	POWER-IN	2.1mm, centre +ve	VIN (nominal +12V)
J33	POWER-IN	4 pin MOLEX	Alternative power in connector (nom. +12V)
J34	POWER-OUT	2 pin MOLEX6410	Header for TBD use
J35-J37	IO-CONFIG	HIROSE FX11-100S	Connectors for IO 'personality' module
CPCI-J1	CPCI		CPCI interface connector – power only

Table 3: List of Connectors

Figure 6-1: GR716-CPCI-DEV Front Panel

P1

EXT_SYSCLK	DGND	1	2	DGND	EXT_SPWCLK
GPIO50	DGND	3	4	DGND	
GPIO52		5	6		GPIO49
GPIO54		7	8		GPIO51
GPIO56		9	10		GPIO53
GPIO58		11	12		GPIO55
GPIO60		13	14		GPIO57
GPIO62		15	16		GPIO59
GPIO0		17	18		GPIO61
		19	20		GPIO63
GPIO2	DGND	21	22	DGND	GPIO1
GPIO4		23	24		GPIO3
GPIO6		25	26		GPIO5
GPIO8		27	28		GPIO7
GPIO10		29	30		GPIO9
GPIO12		31	32		GPIO11
GPIO14		33	34		GPIO13
GPIO16		35	36		GPIO15
		37	38		
GPIO18	DGND	39	40	DGND	GPIO17
GPIO20		41	42		GPIO19
GPIO22		43	44		GPIO21
GPIO24		45	46		GPIO23
GPIO26		47	48		GPIO25
GPIO28		49	50		GPIO27
GPIO30		51	52		GPIO29
GPIO32		53	54		GPIO31
		55	56		
	DGND	57	58	DGND	
		59	60		
	DGND	61	62	DGND	
		63	64		

HDR2X32

P2

	DGND	1	2	DGND	
	+VIN	3	4	+VIN	
RX2_P	DGND	5	6	DGND	RX2_N
RX1_P		7	8		RX1_N
RX0_P		9	10		RX0_N
		11	12		
	DGND	13	14	DGND	TX2_N
TX2_P		15	16		TX1_N
TX1_P		17	18		TX0_N
TX0_P		19	20		
VREFBUF	DGND	21	22	DGND	VREFIN
		23	24		
GPIO48	AGND	25	26	AGND	GPIO47
GPIO46		27	28		GPIO45
		29	30		
GPIO44	AGND	31	32	AGND	GPIO42
GPIO43		33	34		GPIO41
		35	36		
GPIO40	AGND	37	38	AGND	GPIO38
GPIO39		39	40		GPIO37
		41	42		
SPIM_MOSI	AGND	43	44	AGND	SPIM_MISO
SPIM_SEL		45	46		SPIM_SCK
		47	48		
PM_SDA	DGND	49	50	DGND	PM_SCL
RESET_OUT_N		51	52		RESET_IN_N
DSURX		53	54		DSUTX
DSUEN		55	56		DSUBRE
		57	58		
GPIO35	DGND	59	60	DGND	GPIO36
GPIO33		61	62		GPIO34
		63	64		

Table 4: Expansion connector P1 & P2 Pin-out

P3

EXT_SYSCLK	DGND	1	2	DGND	EXT_SPWCLK
	DGND	3	4	DGND	
GPIO50		5	6		GPIO49
GPIO52		7	8		GPIO51
GPIO54		9	10		GPIO53
GPIO56		11	12		GPIO55
GPIO58		13	14		GPIO57
GPIO60		15	16		GPIO59
GPIO62		17	18		GPIO61
GPIO0		19	20		GPIO63
		21	22		
GPIO2	DGND	23	24	DGND	GPIO1
GPIO4		25	26		GPIO3
GPIO6		27	28		GPIO5
GPIO8		29	30		GPIO7
GPIO10		31	32		GPIO9
GPIO12		33	34		GPIO11
GPIO14		35	36		GPIO13
GPIO16		37	38		GPIO15
		39	40		
GPIO18	DGND	41	42	DGND	GPIO17
GPIO20		43	44		GPIO19
GPIO22		45	46		GPIO21
GPIO24		47	48		GPIO23
GPIO26		49	50		GPIO25
GPIO28		51	52		GPIO27
GPIO30		53	54		GPIO29
GPIO32		55	56		GPIO31
		57	58		
	DGND	59	60	DGND	
		61	62		
	DGND	63	64	DGND	

HDR2X32

P4

	DGND	1	2	DGND	
	+VIN	3	4	+VIN	
	DGND	5	6	DGND	
RX2_P		7	8		RX2_N
RX1_P		9	10		RX1_N
RX0_P		11	12		RX0_N
	DGND	13	14	DGND	
TX2_P		15	16		TX2_N
TX1_P		17	18		TX1_N
TX0_P		19	20		TX0_N
VREFBUF	DGND	21	22	DGND	VREFIN
		23	24		
GPIO48	AGND	25	26	AGND	GPIO47
GPIO46		27	28		GPIO45
		29	30		
GPIO44	AGND	31	32	AGND	GPIO42
GPIO43		33	34		GPIO41
		35	36		
GPIO40	AGND	37	38	AGND	GPIO38
GPIO39		39	40		GPIO37
		41	42		
SPIM_MOSI	AGND	43	44	AGND	SPIM_MISO
SPIM_SEL		45	46		SPIM_SCK
		47	48		
PM_SDA	DGND	49	50	DGND	PM_SCL
RESET_OUT_N		51	52		RESET_IN_N
DSURX		53	54		DSUTX
DSUEN		55	56		DSUBRE
		57	58		
GPIO35	DGND	59	60	DGND	GPIO36
GPIO33		61	62		GPIO34
		63	64		

HDR2X32

Table 5: Expansion connector P3 & P4 Pin-out

Pin	Name	Comment
1	VBUS	+5V (from external host)
2	DM	Data Minus
3	DP	Data Plus
4	ID	Not used
5	**DGND**	Ground

Table 6: J1 USB type Micro B connector – FTDI Serial Link

Function	Connector Pin			Function
GPIO0	1	■ □	2	DGND
GPIO1	3	□ □	4	DGND
GPIO2	5	□ □	6	DGND
GPIO3	7	□ □	8	DGND
GPIO4	9	□ □	10	DGND
GPIO5	11	□ □	12	DGND
GPIO6	13	□ □	14	DGND
GPIO7	15	□ □	16	DGND
GPIO8	17	□ □	18	DGND
GPIO9	19	□ □	20	DGND
GPIO10	21	□ □	22	DGND
GPIO11	23	□ □	24	DGND
GPIO12	25	□ □	26	DGND
GPIO13	27	□ □	28	DGND
GPIO14	29	□ □	30	DGND
GPIO15	31	□ □	32	DGND
(+3.3V)	33	□ □	34	DGND

Table 7: J2 GPIO Header Pin out

Function	Connector Pin			Function
GPIO16	1	■	□ 2	DGND
GPIO17	3	□	□ 4	DGND
GPIO18	5	□	□ 6	DGND
GPIO19	7	□	□ 8	DGND
GPIO20	9	□	□ 10	DGND
GPIO21	11	□	□ 12	DGND
GPIO22	13	□	□ 14	DGND
GPIO23	15	□	□ 16	DGND
GPIO24	17	□	□ 18	DGND
GPIO25	19	□	□ 20	DGND
GPIO26	21	□	□ 22	DGND
GPIO27	23	□	□ 24	DGND
GPIO28	25	□	□ 26	DGND
GPIO29	27	□	□ 28	DGND
GPIO30	29	□	□ 30	DGND
GPIO31	31	□	□ 32	DGND
(+3.3V)	33	□	□ 34	DGND

Table 8: J3 GPIO Header Pin out

Function	Connector Pin			Function
GPIO32	1	■	□ 2	DGND
GPIO33	3	□	□ 4	DGND
GPIO34	5	□	□ 6	DGND
GPIO35	7	□	□ 8	DGND
GPIO36	9	□	□ 10	DGND
GPIO37	11	□	□ 12	DGND
GPIO38	13	□	□ 14	DGND
GPIO39	15	□	□ 16	DGND
GPIO40	17	□	□ 18	DGND
GPIO41	19	□	□ 20	DGND
GPIO42	21	□	□ 22	DGND
GPIO43	23	□	□ 24	DGND
GPIO44	25	□	□ 26	DGND
GPIO45	27	□	□ 28	DGND
GPIO46	29	□	□ 30	DGND
GPIO47	31	□	□ 32	DGND
(+3.3V)	33	□	□ 34	DGND

Table 9: J4 GPIO Header Pin out

Function	Connector Pin				Function
GPIO48	1	■	□	2	DGND
GPIO49	3	□	□	4	DGND
GPIO50	5	□	□	6	DGND
GPIO51	7	□	□	8	DGND
GPIO52	9	□	□	10	DGND
GPIO53	11	□	□	12	DGND
GPIO54	13	□	□	14	DGND
GPIO55	15	□	□	16	DGND
GPIO56	17	□	□	18	DGND
GPIO57	19	□	□	20	DGND
GPIO58	21	□	□	22	DGND
GPIO59	23	□	□	24	DGND
GPIO60	25	□	□	26	DGND
GPIO61	27	□	□	28	DGND
GPIO62	29	□	□	30	DGND
GPIO63	31	□	□	32	DGND
(+3.3V)	33	□	□	34	DGND

Table 10: J5 GPIO Header Pin out
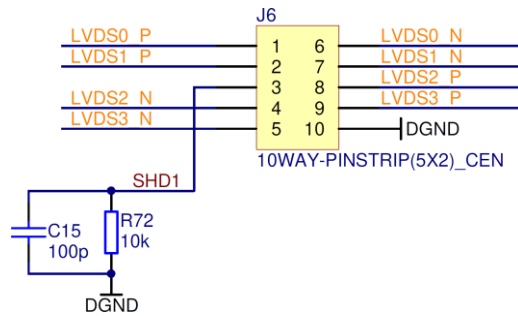
Table 11: J6 SPW/SPI4S Header

(Pins 1-9 connect 1:1 to MDM9S on front panel)
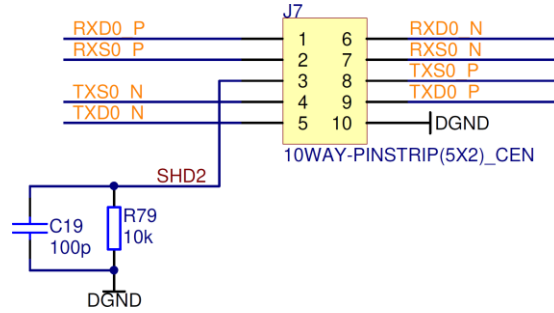
Table 12: J7 SPW-0 Header

(Pins 1-9 connect 1:1 to MDM9S on front panel)
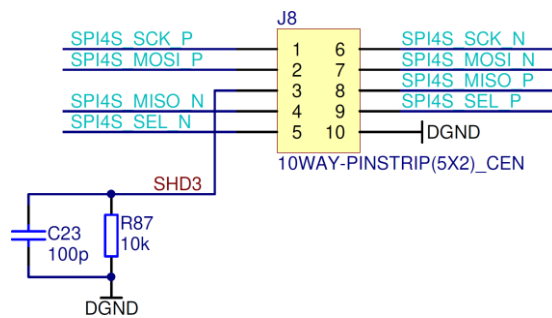
Table 13: J8 SPI4S-R Connector

(Pins 1-9 connect 1:1 to MDM9S on front panel)
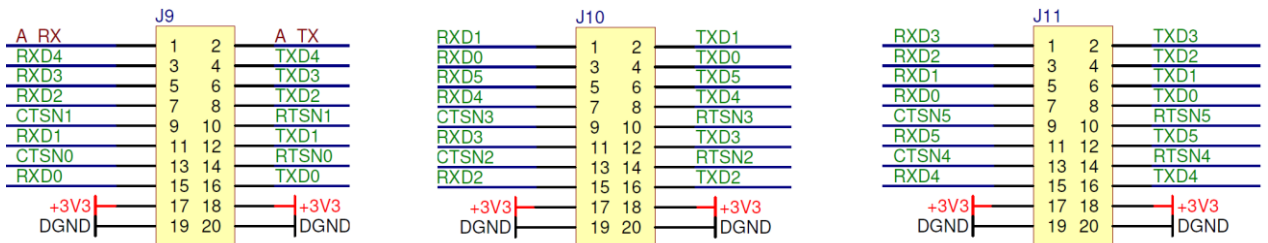
Table 14: J9, J10, J11 UART Interface Headers
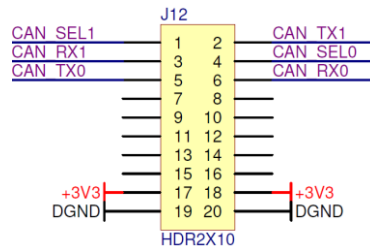
Table 15: J12 CAN Interface Headers
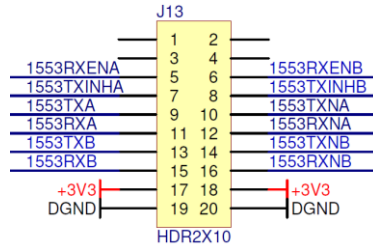
Table 16: J13 CAN Interface Headers
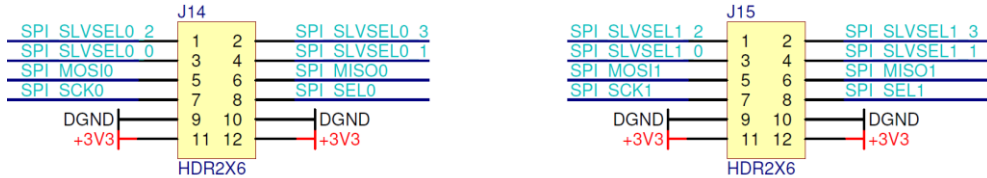
Table 17: J14 & J15 CAN Interface Headers
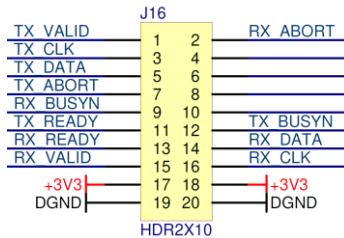
Table 18: J15 PW Interface Headers

Pin	Name	Comment
Inner	SIGNAL	Signal
Outer	AGND	Ground

Table 19: J17-J31 MMCX miniature coax connectors

Pin	Name	Comment
+VE	+VIN	Inner Pin, +5V to +12V, typically 1 A
-VE	DGND	Outer Pin Return

Table 20: J32 POWER – External Power Connector

Pin	Name	Comment
1	+VIN	+VIN (+12V nominal)
2	**DGND**	Ground
3	**DGND**	Ground
4	nc	Not connected

Table 21: J33 POWER – External Power Connector – Alternative

Pin	Name	Comment
1	**DGND**	Ground
2	+VIN	+VIN (+12V nominal)

Table 22: J34 Power-Out connector

J35 (HIROSE-FX11LA-100S/10)

Left signal	Pin	Pin	Right signal
GPIO0	1	100	GPIO1
GPIO2	2	99	GPIO3
GPIO4	3	98	GPIO5
GPIO6	4	97	GPIO7
GPIO8	5	96	GPIO9
DGND	G1	G10	DGND
GPIO10	6	95	GPIO11
GPIO12	7	94	GPIO13
GPIO14	8	93	GPIO15
GPIO16	9	92	GPIO17
GPIO18	10	91	GPIO19
GPIO20	11	90	GPIO21
GPIO22	12	89	GPIO23
GPIO24	13	88	GPIO25
GPIO26	14	87	GPIO27
GPIO28	15	86	GPIO29
DGND	G2	G9	DGND
GPIO30	16	85	GPIO31
GPIO32	17	84	GPIO33
GPIO34	18	83	GPIO35
GPIO36	19	82	GPIO37
GPIO38	20	81	GPIO39
GPIO40	21	80	GPIO41
GPIO42	22	79	GPIO43
GPIO44	23	78	GPIO45
GPIO46	24	77	GPIO47
GPIO48	25	76	GPIO49
DGND	G3	G8	DGND
GPIO50	26	75	GPIO51
GPIO52	27	74	GPIO53
GPIO54	28	73	GPIO55
GPIO56	29	72	GPIO57
GPIO58	30	71	GPIO59
GPIO60	31	70	GPIO61
GPIO62	32	69	GPIO63
	33	68	
	34	67	
	35	66	
DGND	G4	G7	DGND
	36	65	
	37	64	
	38	63	
	39	62	
	40	61	
	41	60	
	42	59	
	43	58	
	44	57	
	45	56	
DGND	G5	G6	DGND
LVDS0_P	46	55	LVDS1_P
LVDS0_N	47	54	LVDS1_N
DGND	48	53	DGND
LVDS2_P	49	52	LVDS3_P
LVDS2_N	50	51	LVDS3_N

J36 (HIROSE-FX11LA-100S/10)

Left signal	Pin	Pin	Right signal
RTSN0	1	100	XPIO0
CTSN0	2	99	XPIO1
TXD0	3	98	XPIO2
RXD0	4	97	XPIO3
CTSN1	5	96	XPIO4
DGND	G1	G10	DGND
RTSN1	6	95	XPIO5
TXD1	7	94	XPIO6
RXD1	8	93	XPIO7
CTSN2	9	92	XPIO8
RTSN2	10	91	XPIO9
TXD2	11	90	XPIO10
RXD2	12	89	XPIO11
CTSN3	13	88	XPIO12
RTSN3	14	87	XPIO13
TXD3	15	86	XPIO14
DGND	G2	G9	DGND
RXD3	16	85	XPIO15
RTSN4	17	84	XPIO16
TXD4	18	83	XPIO17
RXD4	19	82	XPIO18
CTSN4	20	81	XPIO19
CTSN5	21	80	XPIO20
RTSN5	22	79	XPIO21
TXD5	23	78	XPIO22
RXD5	24	77	XPIO23
EXT_PWMCLK	25	76	XPIO24
DGND	G3	G8	DGND
1553RXENA	26	75	XPIO25
1553TXA	27	74	XPIO26
1553RXA	28	73	XPIO27
1553RXNA	29	72	XPIO28
1553TXNA	30	71	XPIO29
1553TXINHA	31	70	XPIO30
1553RXB	32	69	XPIO31
1553RXNB	33	68	XPIO32
1553RXENB	34	67	XPIO33
1553TXB	35	66	XPIO34
DGND	G4	G7	DGND
CLK1553	36	65	XPIO35
1553TXNB	37	64	XPIO36
1553TXINHB	38	63	XPIO37
CAN_TX0	39	62	XPIO38
CAN_RX0	40	61	XPIO39
CAN_SEL0	41	60	XPIO40
CAN_RX1	42	59	XPIO41
CAN_TX1	43	58	XPIO42
CAN_SEL1	44	57	XPIO43
	45	56	XPIO44
DGND	G5	G6	DGND
SPW_RXD	46	55	XPIO45
SPW_RXS	47	54	XPIO46
DGND	48	53	XPIO47
SPW_TXD	49	52	XPIO48
SPW_TXS	50	51	XPIO49

J37 (HIROSE-FX11LA-100S/10)

Left signal	Pin	Pin	Right signal
RX_BUSYN	1	100	XPIO50
RX_CLK	2	99	XPIO51
RX_DATA	3	98	XPIO52
RX_ABORT	4	97	XPIO53
RX_VALID	5	96	XPIO54
DGND	G1	G10	DGND
RX_READY	6	95	XPIO55
TX_VALID	7	94	XPIO56
TX_CLK	8	93	XPIO57
TX_BUSYN	9	92	XPIO58
TX_READY	10	91	XPIO59
TX_DATA	11	90	XPIO60
TX_ABORT	12	89	XPIO61
	13	88	XPIO62
	14	87	XPIO63
	15	86	
DGND	G2	G9	DGND
SPI_SCK0	16	85	SPI_SCK1
SPI_MISO0	17	84	SPI_MISO1
SPI_MOSI0	18	83	SPI_MOSI1
SPI_SEL0	19	82	SPI_SEL1
SPI_SLVSEL0_0	20	81	SPI_SLVSEL1_0
SPI_SLVSEL0_1	21	80	SPI_SLVSEL1_1
SPI_SLVSEL0_2	22	79	SPI_SLVSEL1_2
SPI_SLVSEL0_3	23	78	SPI_SLVSEL1_3
SPI4S_MISO	24	77	SPI4S_MOSI
SPI4S_SCK	25	76	SPI4S_SEL
DGND	G3	G8	DGND
A_RX	26	75	A_TX
	27	74	
xRX0_P	28	73	xTX0_P
xRX0_N	29	72	xTX0_N
DGND	30	71	DGND
xRX1_P	31	70	xTX1_P
xRX1_N	32	69	xTX1_N
DGND	33	68	DGND
xRX2_P	34	67	xTX2_P
xRX2_N	35	66	xTX2_N
DGND	G4	G7	DGND
	36	65	
	37	64	
	38	63	
	39	62	
AGND	40	61	AGND
DAC0	41	60	DAC1
AGND	42	59	AGND
DAC2	43	58	DAC3
AGND	44	57	AGND
	45	56	
DGND	G5	G6	DGND
ADC0	46	55	ADC2
ADC1	47	54	ADC3
AGND	48	53	AGND
ADC4	49	52	ADC6
ADC5	50	51	ADC7

Table 23: J35, J36, J36 Connectors for Interface Configuration

6.2 List of Headers

Name	Function	Type	Description
JP1	RESET/BREAK	2x2 pin 0.1" Header	Conn. to front panel push button switches
JP2	I2C	2x3 pin 0.1" Header	Enable I2C connection to FTDI interface
JP3	UART-0	2x4 pin 0.1" Header	Enable UART-0 connection to FTDI interface
JP4	UART-1	2x4 pin 0.1" Header	Enable UART-1 connection to FTDI interface
JP5	SPI4S	1x2 pin 0.1" Header	Disable SPI4S interface

Table 24: List of Jumpers

6.3 List of Oscillators, Switches and LED's

Name	Function	Description
X1	EXT_PWMCLCK	8 pin DIL socket for TBD MHz 3.3V oscillator
X2	EXT_SYSCLK	8 pin DIL socket for TBD MHz 3.3V oscillator
X3	EXT_SPWCLCK	8 pin DIL socket for TBD MHz 3.3V oscillator
X4	EXT_MIL1553	8 pin DIL socket for TBD MHz 3.3V oscillator
Y1	FTDI clock	12 MHz crystal, SMD soldered

Table 25: List and definition of Oscillators and Crystals

Name	Function	Description
D1A/B-D32A/B	GPIO	64 LED indicators for GPIO signal status
D33A	POWER_3V3	3.3V power good
D33B	RESET_OUT	RESET_OUT signal from *GR716-BOARD*

Table 26: List and definition of PCB mounted LED's

Name	Function	Description
S1	8 pole SPDT DIP switch	Pull-up/Float/Pull-Down Bootstrap settings – see Table 28

Table 27: List and definition of Switches

Name	Function	Description
S1-1	GPIO0	Disable EDAC
S1-2	GPIO17	Bypass Internal Boot PROM
S1-3	GPIO62	Enable Memory Test
S1-4	GPIO63	Redundant Memory available
S1-5	DSUTX	Copy ASW image
S1-6	SPIM_SEL	Boot Source 0
S1-7	SPIM-SCK	Boot Source 1
S1-8	SPIM-MOSI	Remote access/Boot from memory

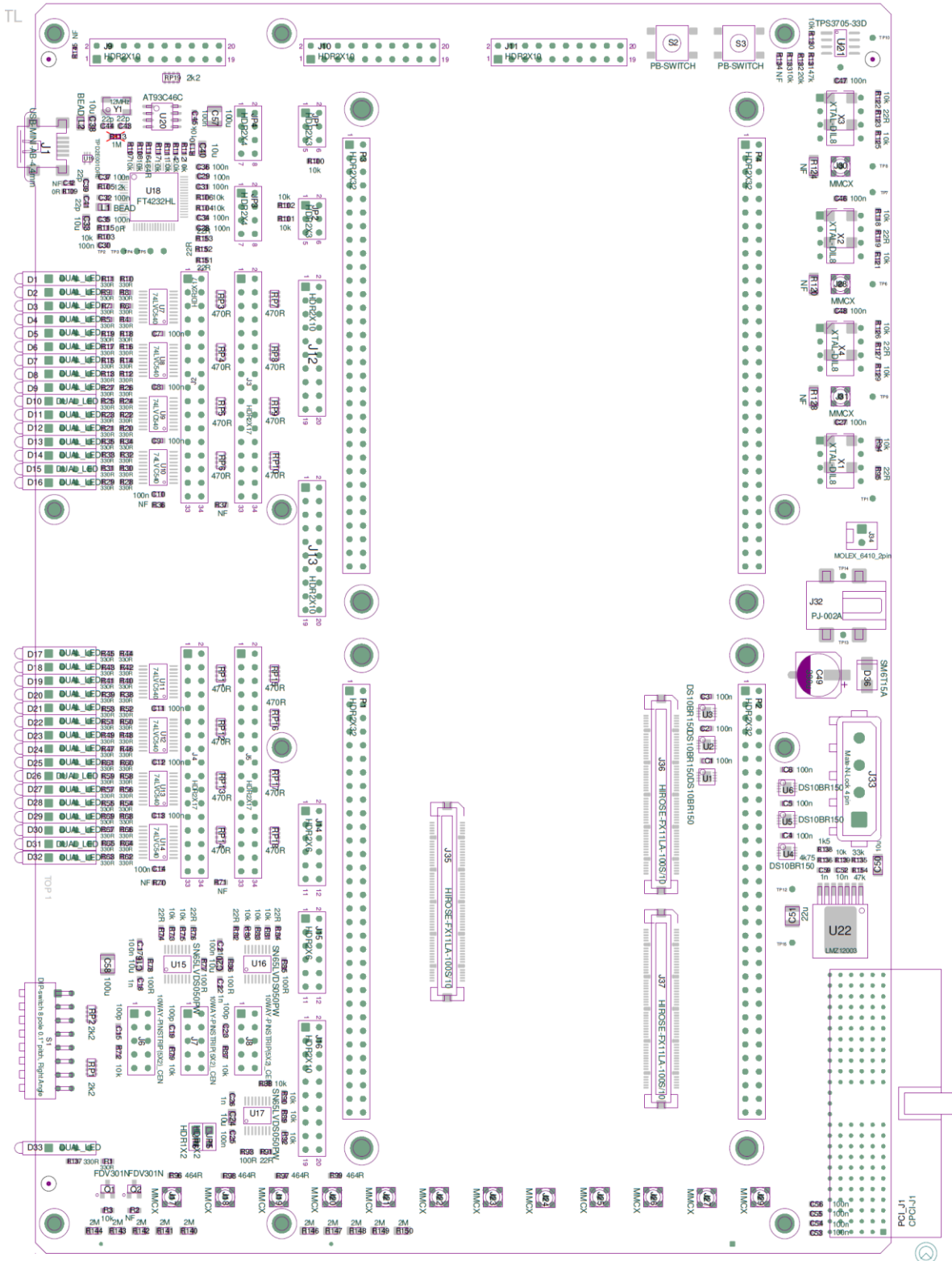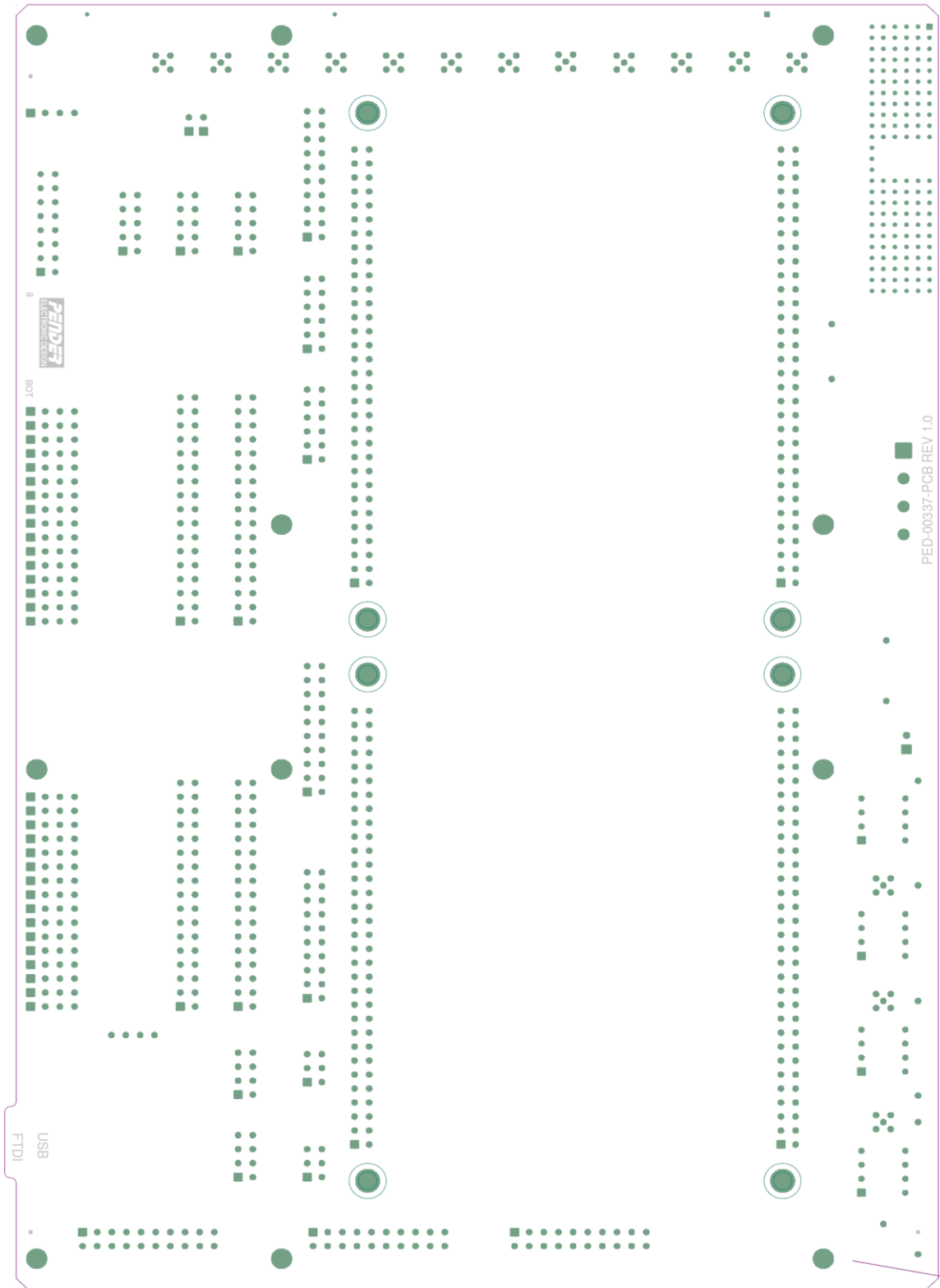*Table 28: Definition of Switch S1 functions*
(refer to [RD1])

Figure 6-2: PCB Top-View

Figure 6-3: PCB Bottom View
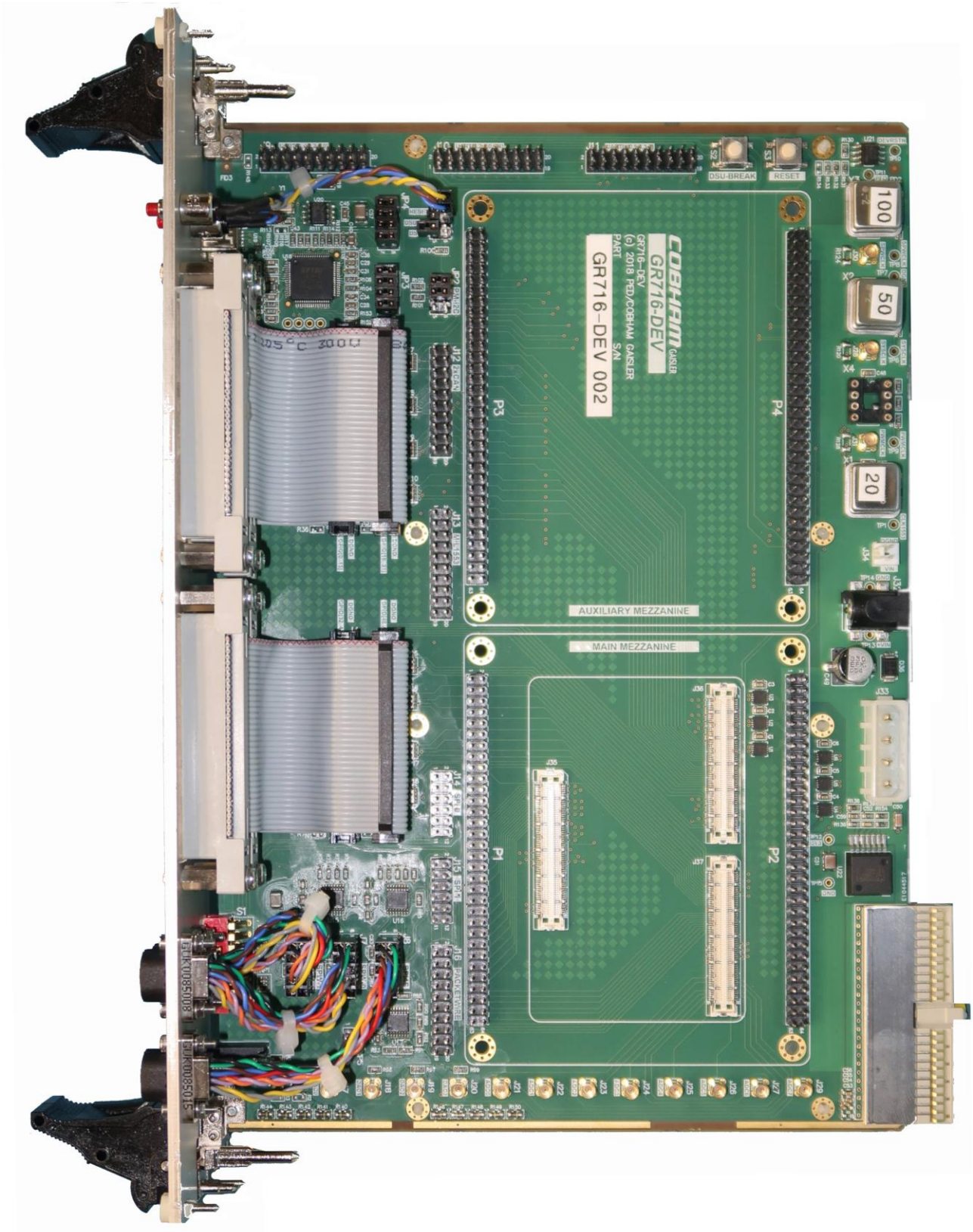
Figure 6-4: PCB Top View (Photo)
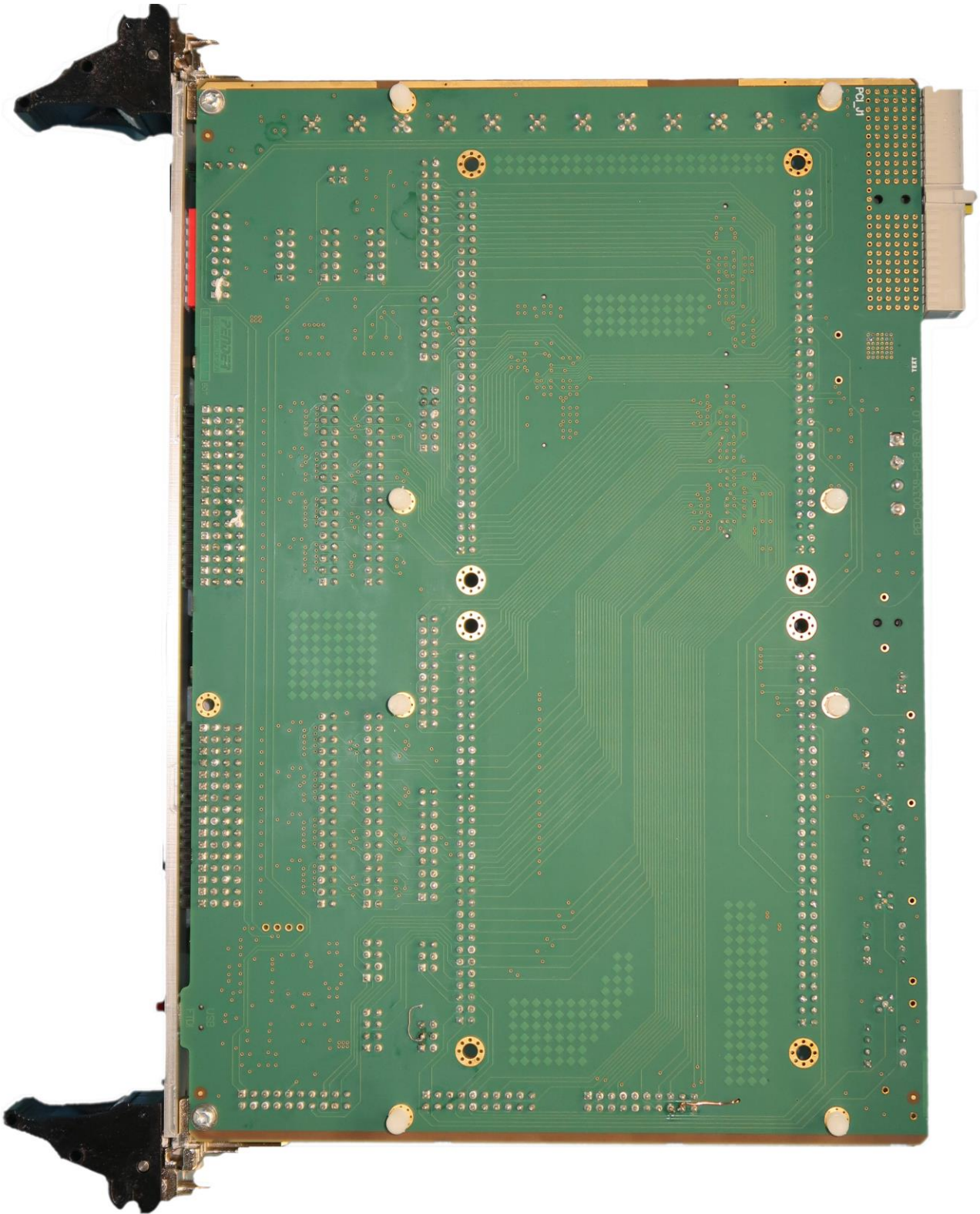
Figure 6-5: PCB Bottom View (Photo)

REVISION INFORMATION

Issue	Date	Section / Page	Description
0.0	2023-10-27	All	Draft Issue
0.1	2019-11-25	4.15	Updated default values
		5	Updated boot start address
		6.3	Updated function for GPIO[0] and GPIO[17]
0.2	2019-05-02	All	Corrected typos
0.3	2020-09-29	All	Corrected name for accessory boards: • GR-ACC-6U-6UART • GR-ACC-GR740
1.0	2023-10-23	All 4.8	Updated company name and template Handling instructions for LVDS added

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Oct 2023, Version 1.0

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Template: GQMS-TPLT-28-1-0 (docx)