

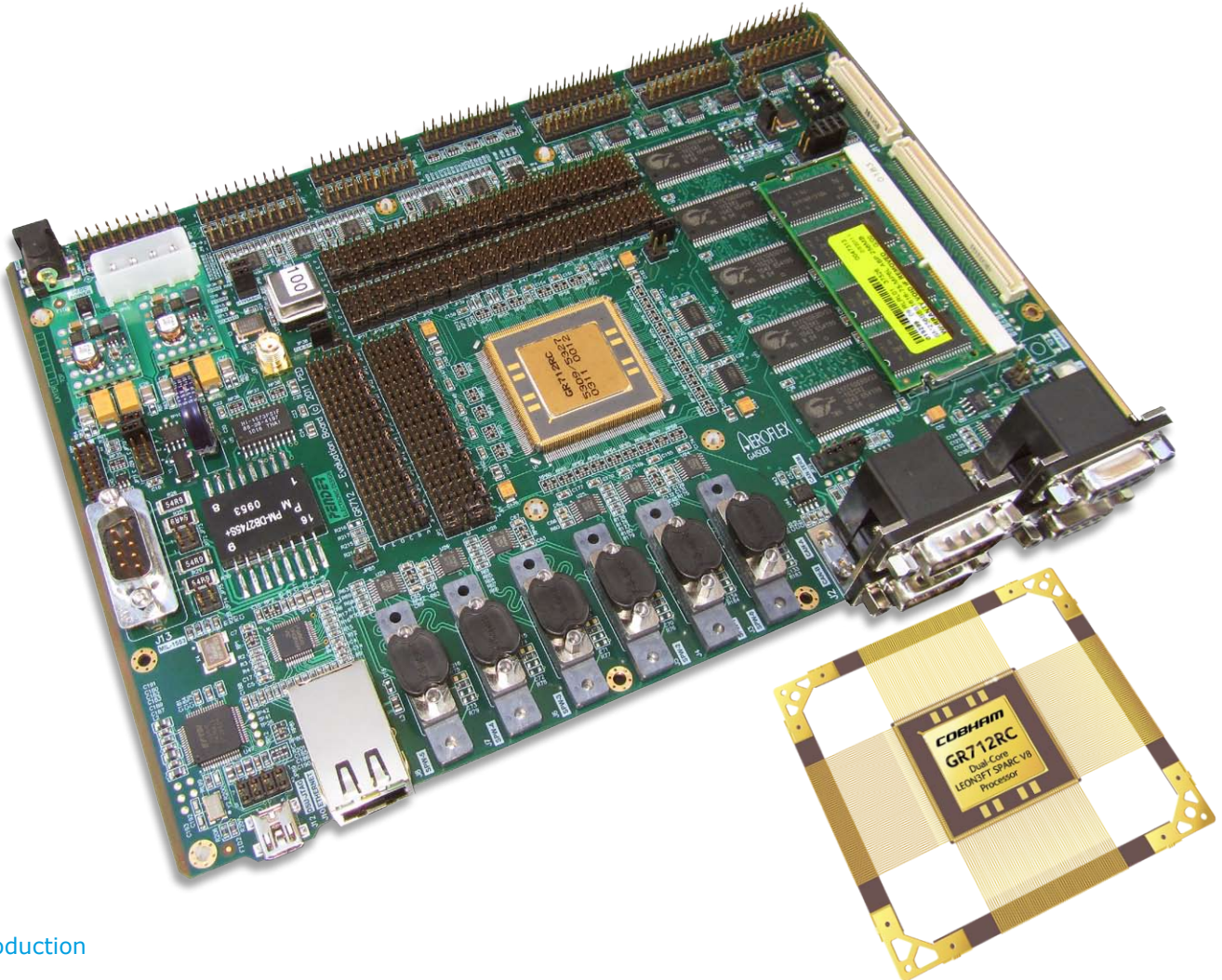
GR712RC Development Board

Dual-Core LEON3-FT Development Board

COBHAM

2017 Product Sheet

The most important thing we build is trust



Introduction

The GR712RC development board has been designed to support the development and fast prototyping of systems based on the Cobham Gaisler GR712RC dual-core 32-bit fault tolerant LEON3FT SPARC V8 processor.

GR712RC is a dual-core LEON3-FT SPARC V8 processor, with advanced interface protocols, dedicated for high reliability Rad-Hard aerospace applications. The GR712RC is fabricated at Tower Semiconductors Ltd.,

using standard 180 nm CMOS technology. It employs radiation-hard-by-design methods from Cobham Gaisler and the RadSafe™ technology from Ramon Chips Ltd., enabling superior radiation hardness together with excellent low-power performance.

The GR712RC development board comprises a custom designed PCB in a Double Eurocard format making the board suitable for stand-alone bench top development, or suitable

for mounting in a housing. The principle interfaces and functions are accessible on the front and back edges of the board.

The GR712RC device incorporates an internal programmable switch matrix which means that the same input/output pin can be used for multiple functions. This board therefore has a large number of configuration features in order to be able to exercise and configure the functions of the device.

GR712RC Development Board

Dual-Core LEON3-FT Development Board
2017 Product Sheet

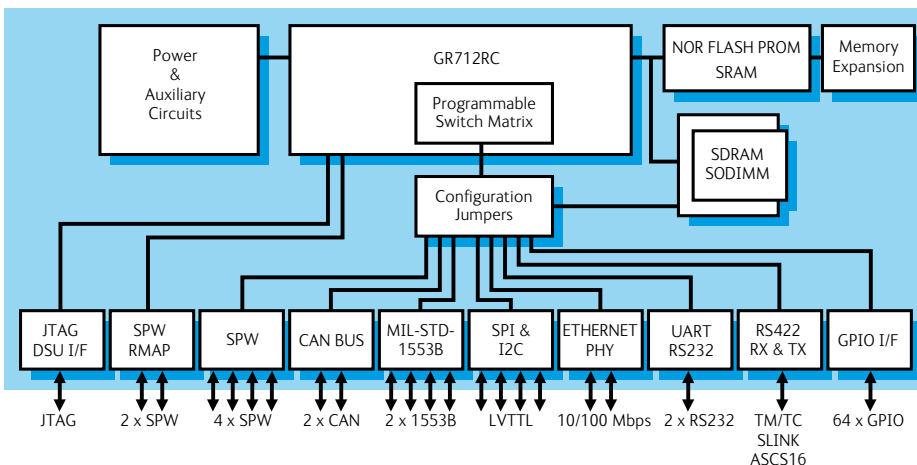
COBHAM

Specifications

- Cobham Gaisler GR712RC in 240-pin Ceramic Quad Flat Package
- Processor core frequency: 100 MHz (SRAM only) (80 MHz with SDRAM)
- Double Eurocard format (233.5 mm x 160 mm)
- On-board power regulation allows stand-alone operation with +5V supply
- JTAG connector for DSU I/F via USB (FT2232HL, USB-MINI-AB connector)
- Six SpaceWire interfaces (LVDS, DS90LV047A/DS90LV048A, MDM9-S)
- Two CAN bus interfaces (ISO11898, DSUB9-P)
- Dual MIL-STD-1553B interface (HI-1573PSI, DSUB9-P)
- SPI master interface on 0.1" headers
- I2C master interface on 0.1" headers
- Ethernet 10/100 Mbps RMII interface (DP83848C, RJ45)
- Switch matrix configuration jumpers for input/output pins
- Two serial UART interfaces (RS232, DSUB9-S)
- 20 RS422 Transmit pairs, on 0.1" headers (DS34LV87)
- 28 RS422 Receive pairs, on 0.1" headers (DS34LV86)
- 26 input and 38 input/output general purpose pins on 0.1" headers
- Memory and user I/O expansion connectors (AMP 5177984-5 120 pin, 5177984-2 80 pin)
- Standard memory options:
 - SDRAM, 144 pin SODIMM (64 bit, 256 Mbyte) (128 Mbyte data & 64 Mbyte checksum)
 - SRAM, on-board 80 Mbit (1 bank x 2 Mword x 40 bit, 10 ns) (optional second bank not fitted as standard)
 - NOR FLASH PROM, on-board 64 Mbit (8 Mword x 8 bit, 90 ns)

Features

- GR712RC dual-core 32-bit fault tolerant LEON3-FT SPARC V8 processor
- On-board memory:
 - SDRAM SODIMM module
 - SRAM
 - NOR FLASH PROM
 - Additional memory via memory expansion connectors
- Interfaces at front edge of board:
 - JTAG debug interface
 - Six SpaceWire interfaces
 - Two CAN bus interfaces
 - Ethernet 10/100 Mbps RMII interface
 - Two serial UART interfaces
- Power, reset, clock and auxiliary circuits
- Interfaces at back edge of board:
 - 26 input and 38 input/output general purpose pins
 - +5 V power connector
- Interfaces on-board:
 - Dual MIL-STD-1553B communication interface
 - I2C master interface
 - SPI master interface



Online resources

<http://gaisler.com/GR712RC>

For further information please contact:

Cobham Gaisler AB
Kungsgatan 12
41119 Göteborg
SWEDEN
Tel: +46-31-7758650
Fax: +46-31-421407