LEON Processor Cache Controller Errata: Instruction Treated as Noncacheable Due to HCACHE Timing

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Technical note

2015-10-27

Doc. No GRLIB-TN-0005

Issue 1.0

CHANGE RECORD

Issue	Date	Section / Page	Description
1.0	2015-10-27		First issue under this document name. This document replaces the document LEON3-HCACHE-ERRATA (latest released version was issue 1 revision 2).

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1 INTRODUCTION

1.1 Scope of the Document

This document describes a design errata in certain versions of the LEON3 and LEON3FT processors when used together with a memory controller that drives the HCACHE AMBA side-band signal with a nonconstant value to signal cacheability of different memory areas. The impact of the error, which versions are affected, and possible workarounds are described.

1.2 Distribution

LEON3 and LEON3FT users are free to use the material in this document in their own documents and to redistribute this document. Please contact Cobham Gaisler for inquires on other distribution.

1.2.1 Contact

For questions on this document, please contact Cobham Gaisler support at support@gaisler.com. When requesting support include the part name if the question is a specific device or the full GRLIB IP library package name if the question relates to a GRLIB IP library license.

2 AFFECTED PRODUCTS

2.1 General

This errata applies to some LEON3/LEON3FT-based devices made using GRLIB revisions earlier than revision b4101.

2.2 Aeroflex components

Aeroflex components/products affected are:

- UT699
- LEON3FT-RTAX Subset of devices affected, contact Aeroflex Gaisler Support

Aeroflex components **NOT** affected are:

- GR712RC NOT affected, processor configuration immune from errata
- UT699E NOT affected, made from a newer revision of GRLIB
- UT700 NOT affected, made from a newer revision of GRLIB
- LEON4-N2X NOT affected, made from a newer revision of GRLIB

2.3 How to check if a design is affected

If you are licensing GRLIB for use in your own FPGA or ASIC design, you can check the following conditions in the design's VHDL source to see if the erratum applies to your system:

1. Check the GRLIB revision. This can be seen in the file name of the downloaded release package, in the directory name after unpacking the release, and in the file lib/grlib/stdlib/version.vhd in the release file tree (constant grlib_build). If this is higher than 4101, you are NOT affected by this error. Otherwise, continue with the following step.
2. Check if you are using a memory controller that toggles the HCACHE AMBA sideband signal. This is the case for most memory controllers in GRLIB that supports a memory-mapped IO area, such as MCTRL and FTMCTRL. If you have a memory controller that drives a constant value on the HCACHE output then you are NOT affected by this error. Otherwise continue with the following step.
3. Check the configuration of the VHDL generic *cached* on the LEON3 processor
    - Designs with GRLIB build ID 2694 are affected by the bug
    - Designs with GRLIB build ID 2695 – 4100 where the *cached* VHDL generic is 0 are affected by the bug.
    - Designs with GRLIB build ID 2695 – 4100 where the *cached* VHDL generic is nonzero are NOT affected by the bug.

3 IMPACT

On systems where the errata is applicable and not using any of the workarounds described in this document, the impact is suboptimal behaviour of the instruction cache in the case of back-to-back fetch after an IO area access. When an instruction is fetched back-to-back with an access to the memory controller's memory-mapped IO area, it will not get its valid bit set when written into the instruction cache and will therefore be fetched again the next time it is executed. The fetched instruction will still be executed correctly, so the impact is on execution timing only.

The errata does not affect applications where the uncacheable (memory-mapped I/O) area of the memory controller is never accessed. An upper bound on the impact is one extra instruction cache miss per performed IO area read or write. This errata is primarily a concern for applications doing a large number of memory-mapped I/O reads or writes in a loop where the loop code may not become properly cached and therefore execute slower than expected.

4 ERRATA DESCRIPTION

The underlying reason for the problem is that the AMBA side-band signal HCACHE generated by the memory controller changes one cycle too late when you perform a PROM/SRAM/SDRAM access (where the memory controller drives HCACHE=1) back-to-back after an IO access (where the memory controller drives HCACHE=0). This makes the LEON3 instruction cache not write in the first word into cache.

This only affects instruction fetches and not data fetches, because for design reasons the processor does not use the HCACHE signal for data fetches (it uses the static AMBA plug'n'play information instead). The only impact of this bug that has been identified is that an instruction fetch immediately after an access to an I/O area will not be stored in cache. The instruction will still be executed correctly, the impact is timing only.

5 SOLUTIONS

5.1 Workaround: Dry-run

One software workaround for the problem is to perform a dry-run through any code that accesses the memory-mapped IO area of the memory controller. During the first run of the code, the read/write access should be performed to a cacheable area, such as the SRAM area, to ensure that this errata does not trigger and any fetched instructions are written correctly into the instruction cache. The pointer to the SRAM area is then swapped with the pointer to the IO area and the same instructions are re-run from cache, avoiding the back-to-back code fetch.

5.2 VHDL correction

If you have access to the RTL sources of the design then the timing of the HCACHE signal can be corrected. Please contact Aeroflex Gaisler support for additional details.