Interfacing the RAD1419 A/D converter with the GRLIB IP core library

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1 INTRODUCTION

1.1 Scope of the Document

The RAD1419 is a 1µs, 800kSPS, 14-bit sampling Analog-to-Digital Converter (ADC) suitable to interface with ASIC and FPGA designs based on the GRLIB IP core library. Three different solutions are proposed to control the ADC using the GRADCDAC - ADC / DAC Interface IP core.

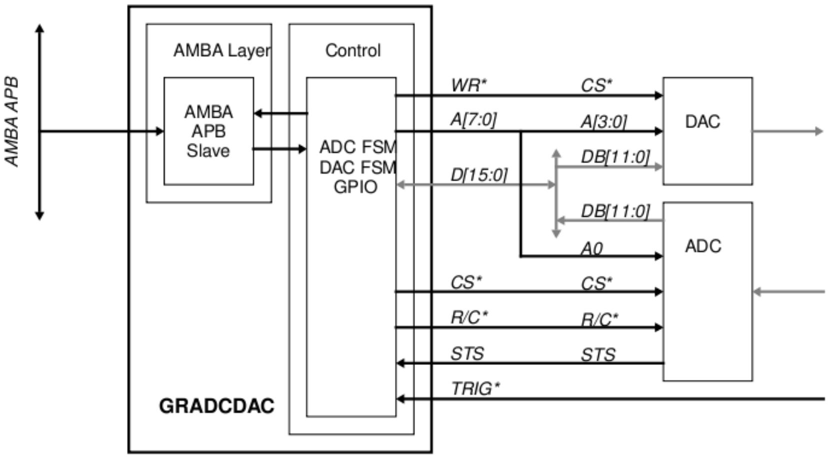

Figure 1: Block diagram and interface of the GRADAC IP core

The first solution consists of using the GRADCDAC controller “as is” in a processor IRQ driven design. The following steps are necessary for sample acquisition:

- Initiate a conversion by an APB write cycle to the GRADCDAC controller
- The GRADCDAC controller generates a processor interrupt once the conversion finishes
- Read the GRADCDAC data register by an APB read cycle in the interrupt routine.

This approach adds the delay of processor interrupt handling and at least two APB transfer cycles to the conversion time and is thus only suitable for selective A-D conversions at low speed.

The second solution is DMA driven, and a GPTIMER core is used to initiate conversion by the GRADCDAC trigger input. Signal acquisition occurs as follows:

- Configure the desired sample rate in the timer
- Configure base address and sample count to the DMA
- Samples are transferred by DMA to a dedicated FTAHBRAM IP core
- Once the sample count is reached a processor interrupt is generated.

This approach allows for a fixed sample rate, and the full ADC bandwidth can be reached. A FTAHBRAM core and a new dedicated DMA core including a GPTIMER has to be added to the design.

Finally, a bare interface solution is proposed, which gives the user a maximum of flexibility on processing data acquired by the ADC. The GRADCDAC front-end is used to control the ADC and to initiate conversion in one of the two provided ways, while sample data is latched into the GRADCDAC and forwarded to user specific logic for further processing.

1.2 Reference Documents

[bcc] Cobham Gaisler: Bare-C Cross-Compiler User’s Manual.
http://www.gaisler.com/doc/bcc.pdf
[grlib] Cobham Gaisler: GRLIB IP Library User’s Manual.
http://www.gaisler.com/products/grlib/grlib.pdf
[1419] Cobham Semiconductor Solutions: RAD1419 Analog-to-Digital Converter Data Sheet.
http://www.aeroflex.com/ams/pagesproduct/datasheets/rad/Datasheet_RAD1419ADC.pdf
[grip] Cobham Gaisler: GRLIB IP Core User’s Manual.
http://www.gaisler.com/products/grlib/grip.pdf

2 ABBREVIATIONS

AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
ASIC	Application Specific Integrated Circuit
CS	Chip Select
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input/Output
IP	Intellectual Property
kSPS	Kilo-Samples

3 PROCESSOR INTERRUPT DRIVEN DESIGN

3.1 Architecture overview

Figure 2 outlines the architecture of the processor interrupt driven design.

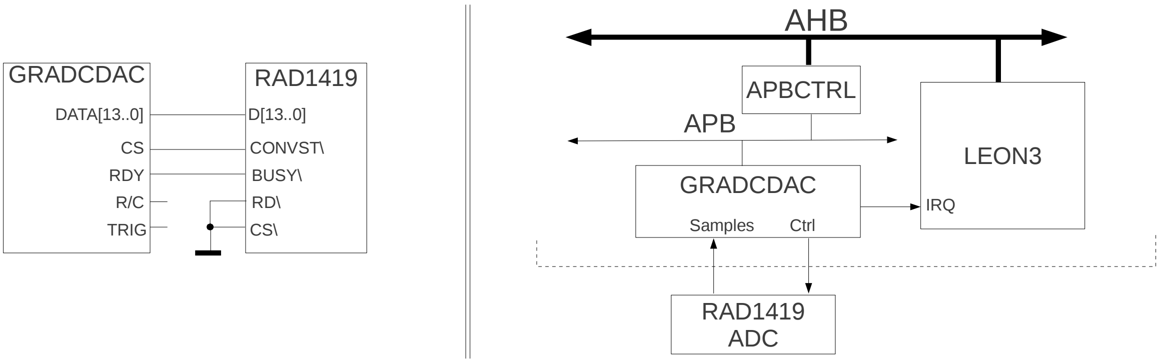

Figure 2: Wiring and architecture overview of the processor interrupt driven design

Note that the ADC CS\ input may be controlled by a GPIO (e.g. the GRADCDAC address interface if unused) in order to take advantage of the different sleep modes of the RAD1419 ADC.

Conversion is initiated by writing to the GRADCDAC Data Input Register *ADIN*. An interrupt handler has to be installed in software to read out the Data Input register. The GRADCDAC status register may also be read out in order to check for possible conversion errors.

Detailed information about installing an interrupt handler in software is described in [bcc], while hardware interrupt steering is outlined in [grlib].

3.2 Configuration

The GRADCDAC configuration register must be set according to the ADC interface and the intended use. The following values are necessary:

- ADCWS: 00000b
  For a system frequency up to 50 MHz no additional wait states are necessary. Timing t_8 (delay between conversions) in [1419] being the limiting factor,
- CSMODE: 11b
  ADC chip select is asserted during conversion and read phase
- CSPOL: 00b
  Polarity of ADC chip select is active low
- RDYMODE: 01b
  Data ready signal is used
- RDYPOL: 1b
  Polarity of ADC ready is rising edge
- TRIGMODE: 00b
  ADC trigger inputs are not used

- ADCDW: 10b
  ADC data with is 16bit (only 14 bit are used)

For full documentation of the GRADCDAC configuration and status registers refer to [grip], chapter 45.4.

3.3 Performance

In addition to the ADC conversion time of about 1200ns, at least two APB accesses and a processor interrupt occur on each conversion. Since the interrupt handling time largely dominates the conversion time, the achievable conversion bandwidth can be seen as practically equal to the maximum handleable interrupt frequency by the processor. Under realistic circumstances the maximum handleable interrupt frequency is expected in the order of 1000/sec. Additionally, this approach is not suitable for signal acquisition since the delay between conversions is not deterministic.

4 DMA DRIVEN DESIGN

4.1 Architecture overview

Figure 3 outlines the architecture of the DMA driven design.

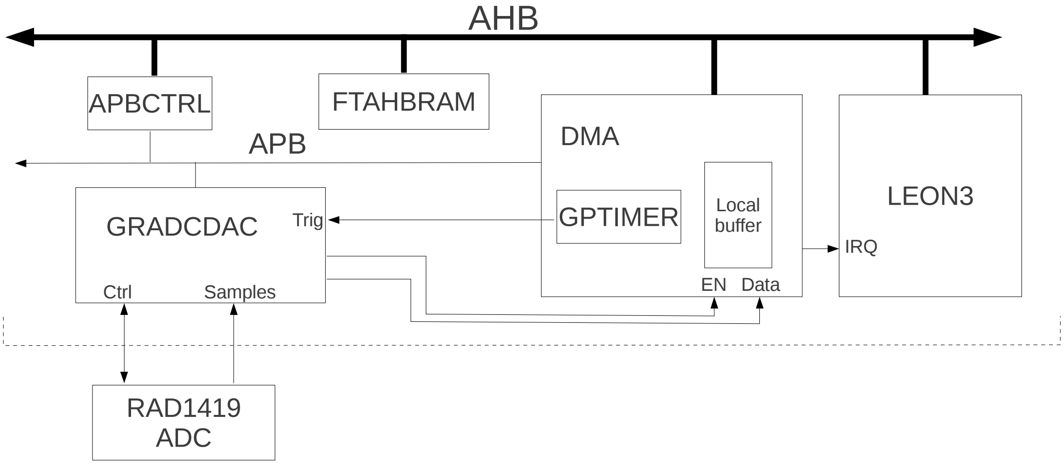

Figure 3: Architecture overview of the timer based design

Signal conversion consists of the following steps:

1. GRADCDAC initialization
2. Programming a sampling rate in the timer
3. Programming a base address (FTAHBRAM location) and sample count in the DMA. This activates a circular write pointer to the internal buffer. The write pointer is incremented on the Data Ready signal, which is forwarded from the ADC by the GRADCDAC.
4. Once the circular buffer has reached a certain fill state, data is written in burst mode to the FTAHBRAM

5. Once the sample count is reached, the DMA triggers a processor interrupt.

4.2 Configuration

Configuration of the GRADCDAC configuration register is the same as in Paragraph 3.2, except

- TRIGMODE: 01b
  ADI.TRIG[0] is used as trigger source.
- TRIGPOL: 1b
  Trigger on rising edge

Note that the ADC CS\ input may be controlled by a GPIO (e.g. the GRADCDAC address interface if unused) in order to take advantage of the different sleep modes of the RAD1419 ADC.

4.3 Performance

This design allows to immediately trigger a new conversion after completion of the previous one. However, the GRADCDAC state-machine imposes five clock cycles between conversion end and accepting a new trigger event. On systems running at lower clock speed this delay affects increasingly the maximum sample rate. For example, at 25 MHz system clock this leads to a sampling rate of about 650 kSamples per second. In order to overcome this limitation, the GRADCDAC could be run in open-loop conversion mode, which operates without use of the RDY signal. However, the core has to be adapted for this purpose since the configuration of open-loop conversion timing is at multiples of 512 clock cycles when using the design as-is.

4.4 Design considerations

The DMA/local buffer should implement a status register which reflects the status of the completed sampling period (i.e. transfer of programmed number of samples to the FTAHBRAM). In particular, a possible buffer overflow has to be signaled to the processor, which may check the status register in the interrupt routine.

Another possible conversion error would be to exceed the supported ADC sampling rate. This may easily occur since the conversion triggering timer is freely programmable. However, the current design of the GRADCDAC foresees access to the corresponding ADSTAT status register by APB. In order to enable the DMA/local buffer to check for and handle such errors instantly, at least the ADCTO (ADC conversion timeout) and ADCNO (ADC conversion request rejected due to ongoing ADC or DAC conversion) fields of the ADSTAT register should be directly forwarded to the DMA/local buffer.

The expected available AHB bandwidth in a given system must be taken into consideration in order to allow to purge the the local buffer in a timely manner. In an example system where the DMA performs burst writes of 8 words, the circular buffer could be implemented with N*8 words, where N>=2. Depending on AHB arbitration mode, the number of masters on the bus and the expected temporal distribution of AHB transfers in the system, a higher value of N could be chosen to minimize the chance of a buffer overflow due to AHB congestion.

5 BARE INTERFACE DESIGN

Figure 4 outlines the architecture of a bare interface solution.

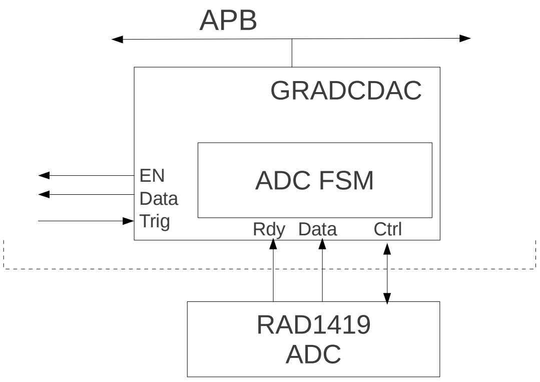

Figure 4: Architecture overview of a bare interface design

In this configuration the user takes advantage of the GRADCDAC controller FSM to initiate conversion, but has full flexibility on how to handle the incoming samples.

Wiring will be the same as for the interrupt based approach, while additional interfaces have to be added to connect with the user design.

Conversion can be triggered either by one of the GRADCDAC trigger inputs or by writing to its Data Input Register [ADIN] . The TRIGMODE and TRIGPOL registers have to be set accordingly.

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