LEON3 NANDFCTRL2

LEON3-XCKU-NANDFCTRL2-EX-UM

Features

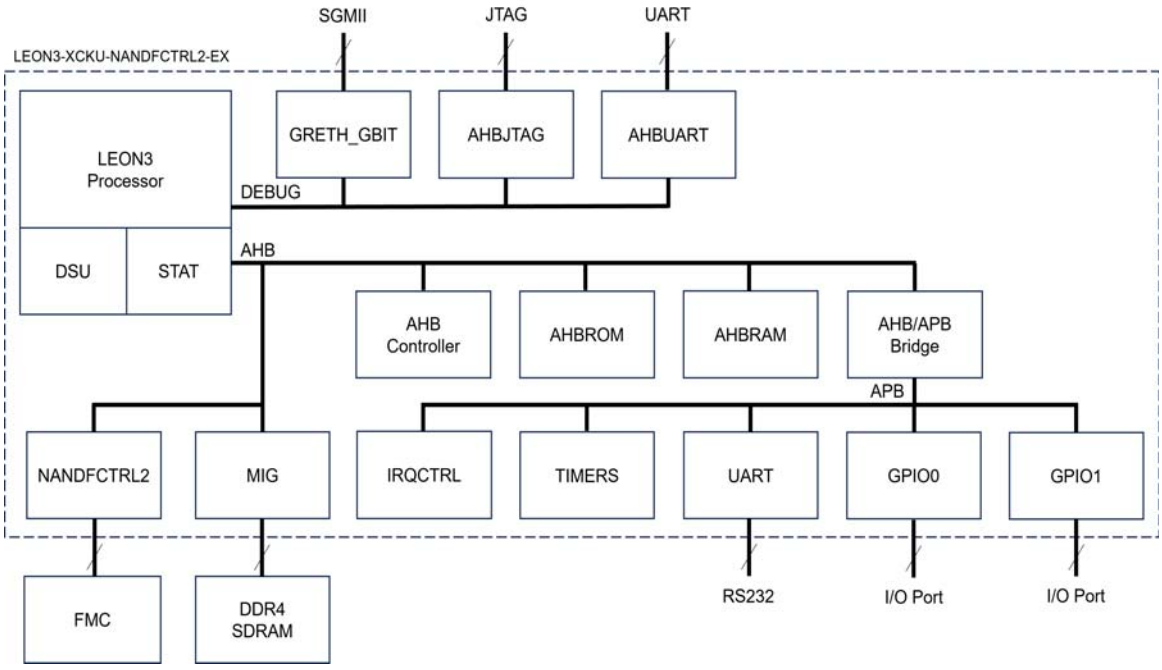
- LEON3 SPARC V8e integer unit
  16 KiB instruction and
  16 KiB data caches,
  hardware multiplier and
  divider, power-down mode, etc.
- NANDFCTRL2 NAND FLASH controller
- Advanced on-chip debug support unit with UART, JTAG and Ethernet links.
- DDR4 SDRAM
- UART, Timers, GPIO port, Interrupt controller, Status registers
- Ethernet 10/100/1000 Mbit MAC interface

Description

The LEON3-XCKU-NANDFCTRL2 example bitstream consist of a LEON3 example design including NANDFCTRL2 using a template design for Xilinx Kintex Ultrascale devices. The bitstream are suitable to evaluate NANDFCTRL2 together with a NAND FLASH Memory FMC mezzanine board.

Specification

- Targets Xilinx Kintex Ultrascale KCU105 Evaluation Kit FPGA board
- 100 MHz system frequency



Applications

The LEON3-XCKU-NANDFCTRL2 example bitstream can be used to evaluate NANDFCTRL2 interfacing a NAND FLASH device on a FMC mezzanine board on a Xilinx Kintex Ultrascale development board.

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1 Introduction

1.1 Scope

The GRLIB IP library includes NANDFCTRL2 - a NAND FLASH memory controller designed to operate with ONFI 4.0 FLASH memory devices. The core implements a BCH EDAC with the capability of correcting up to 60 errors per chunk of 1024 bytes of data. Other features includes DMA, a data randomizer and a Ready/Busy timeout block.

The LEON line of processors and the GRLIB IP library has support for Xilinx Kintex Ultrascale devices. This support consists of a techmap layer that wraps specific technology elements such as memory macros and pads. GRLIB also contains a template designs for development boards such as the Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit and infrastructure that automatically builds project files for Xilinx Vivado and synthesis tools such as Mentor Precision Hi-Rel and Synopsys Synplify Premier.

This document describes a ready-made FPGA configuration (bitstream) that have been built from the GRLIB template design with the purpose to evaluate the NANDFCTRL2 interfacing a NAND FLASH device mounted on a FMC mezzanine.

More information about NANDFCTRL2 is available at https://www.gaisler.com/NANDFCTRL2

1.2 Document revision history

Table 1. Change record

Version	Date	Note
1.0	2023 September	First issue

1.3 Reference documents

[AMBA] AMBA™ Specification, Rev 2.0, ARM IHI 0011A, 13 May 1999, Issue A, first release, ARM Limited

[GRLIB] GRLIB IP Library User's Manual, Frontgrade Gaisler, www.gaisler.com

[GRIP] GRLIB IP Core User's Manual, Frontgrade Gaisler, www.gaisler.com

[QSG] LEON3-XCKU-NANDFCTRL2-EX Quick Start Guide, LEON3-XCKU-NANDFCTRL2-EX-QSG, https://www.gaisler.com/NANDFCTRL2

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2 Example designs

2.1 Overview

LEON3-XCKU-NANDFCTRL2-EX design is centered around the AMBA [AMBA] Advanced High-speed Bus (AHB), to which the processor(s) and other high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge. The architecture for the basic design is shown in figure 1.

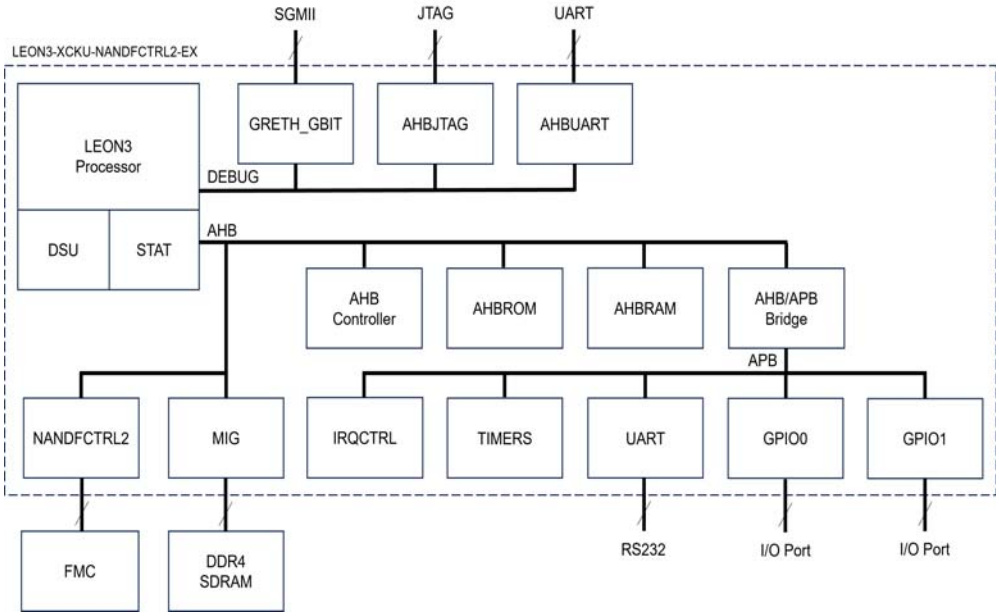

Figure 1. Architectural block diagram of LEON3-XCKU-NANDFCTRL2-EX

Please also note that while not shown in the block diagram above, the Ethernet controller (GRETH_GBIT) is also connected to the main AHB bus and not only the Debug AHB bus.

The LEON3-XCKU-NANDFCTRL2-EX architecture includes the following modules:

- LEON3 SPARC V8e Integer Unit with 16 KiB instruction cache and 16 KiB data cache.
- LEON3 Statistics unit.
- Debug Support Unit with UART, Ethernet, and JTAG Debug Links.
- NANDFCTRL2, NAND FLASH memory controller.
- Xilinx MIG DDR4 SDRAM controller.
- Timer unit with two 32-bit timers.
- Interrupt controller for 15 interrupts in two priority levels.
- UART with FIFO and separate baud rate generator.
- 2 General purpose I/O port (GPIO).

The GRLIB IP library contains a template design that has been used as the base for the LEON3-XCKU-NANDFCTRL2-EX design. The template design can easily be extended to add additional GRLIB IP library IP cores such as:

- Memory controllers with EDAC
- SpaceWire links with CRC support and hardware RMAP target
- SpaceFibre links
- CAN-2.0 controllers
- Mil-Std-1553 BC/BM/RT

A full list of GRLIB IP library components can be found in [GRIP]. The GRLIB user's manual is available on-line [GRLIB].

2.2 Configurations

To get access to the bitstream, contact sales@gaisler.com.
For more information about NANDFCTRL2 visit https://www.gaisler.com/NANDFCTRL2

The table below presents the setting of the implementation parameters used to configure NANDFCTRL2 for the LEON3-XCKU-NANDFCTRL2-EX design.

Table 2. Example configurations

NANDFCTRL2 Implementation parameter	**Value**
nrofce	4
nrofch	2
nrofrb	4
rnd	1
mem0_data	16384
mem0_spare	2208
mem0_ecc_sel	0
mem1_data	*8192*
mem1_spare	*448*
mem1_ecc_sel	*1*
mem2_data	*4096*
mem2_spare	*224*
mem2_ecc_sel	*1*
ecc0_gfsize	14
ecc0_chunk	1024
ecc0_cap	60
ecc1_gfsize	*13*
ecc1_chunk	*512*
ecc1_cap	0

Note: The configuration above targets one specific flash memory device and only instantiate one ecc block (ecc1_cap = 0) which implies that the mem1, mem2 and ecc1 values are not important.

3 Architecture

3.1 Cores

The common architecture is based on cores from the GRLIB IP library. The vendor and device identifiers for each core can be extracted from the plug & play information. The used IP cores are listed in table 3.

Table 3. Used IP cores

Core	Function	Vendor	Device
LEON3	LEON3 SPARC V8 32-bit processor	0x01	0x003
DSU3	LEON3 Debug support unit	0x01	0x004
L3STAT	LEON3 Performance counters	0x01	0x098
AHBCTRL	AHB Arbiter & Decoder	0x01	-
APBCTRL	AHB/APB Bridge	0x01	0x006
IRQMP	LEON3 Interrupt controller	0x01	0x00D
GPTIMER	Modular timer unit with watchdog	0x01	0x011
AHBUART	Serial/AHB debug interface	0x01	0x007
AHBJTAG	JTAG/AHB debug interface	0x01	0x01C
GRETH_GBIT	GR Ethernet MAC with debug interface	0x01	0x01D
NANDFCTRL2	NAND Flash Controller	0x01	0x0C5
APBUART	8-bit UART with FIFO	0x01	0x00C
Xilinx MIG	Xilinx DDR4 MIG - with GRLIB wrapper	0x01	0x090
GRGPIO	General purpose I/O port	0x01	0x01A
AHBRAM	Single-port AHB SRAM module	0x01	0x00E
AHBROM	Single-port ROM with AHB interface	0x01	0x01B
Xilinx SGMII	Xilinx SGMII Interface - with GRLIB wrapper	0x01	0x092

3.2 Interrupts

The LEON3-XCKU-NANDFCTRL2-EX use interrupt assignment according to the table below. See the description of the individual cores for how and when the interrupts are raised. All interrupts are handled by the interrupt controller and forwarded to the processor.

Table 4. Interrupt assignment

Core	Interrupt	Comment
NANDFCTRL2	4	
GRETH_GBIT	5	
APBUART	2	
GPTIMER	8	
SGMII	11	

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3.3 Memory map

The memory map shown in table 5 is based on the AMBA AHB address space. An access to addresses outside ranges will receive an AHB error response. The detailed register layout is defined in the description of each core.

Table 5. AMBA AHB address range

Core	Address range	Area
AHBROM	0x00000000 - 0x000FFFFF	ROM area
Xilinx MIG - AHB	0x40000000 - 0x4FFFFFFF	DDR4 SDRAM Area
APBUART	0x80000100 - 0x800001FF	Registers
GPTIMER	0x80000300 - 0x800003FF	Registers
Xilinx MIG - APB	0x80000400 - 0x800004FF	Registers
AHBUART	0x80000700 - 0x800007FF	Registers
GPIO (0)	0x80000A00 - 0x80000AFF	Registers
GPIO (0)	0x80000B00 - 0x80000BFF	Registers
NANDFCTRL2	0x80000C00 - 0x80000DFF	Registers
Xilinx SGMII	0x80001000 - 0x80001FFF	Registers
L3STAT	0x80010000 - 0x800103FF	Registers
GRETH_GBIT	0x800C0000 - 0x800FFFFF	Registers
AHBRAM	0xA0000000 - 0xA0100000	Registers
DSU	0xD0000000 - 0xDFFFFFFF	Registers
AHB plug&play	0xFFFFF000 - 0xFFFFFFFF	ROM area

3.4 IP core documentation

This user manual does not contain IP core documentation. Please refer to the GRLIB IP Core User's Manual [GRIP] available at http://gaisler.com/products/grlib/grip.pdf.

The GRMON debug monitor also provides information about the system-on-chip's configuration via the command **info sys**.

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3.5 Signals

Please see the LEON3-XCKU-NANDFCTRL2-EX Quick Start Guide [QSG] for information on FPGA pinout.

3.6 Resource utilization

Resource utilization is described in the GRLIB area spreadsheet, available at:

https://www.gaisler.com/products/grlib/grlib_area.xls

4 Working with the board

4.1 Prerequisites

The following items are required to use LEON3-XCKU-NANDFCTRL2-EX design:

- Xilinx KCU105 Evaluation Kit
- LEON3-XCKU-NANDFCTRL2-EX bitstream with example applications.
- Frontgrade UT81NDQ512G8T NAND FLASH FMC mezzanine board:

  `PN UT81NDQ512G8T-KU060-EVB`

  Contact your local Frontgrade representative for inquiries.
- Xilinx Vivado Design Suite (to program the FPGA). Vivado is available at https://www.xilinx.com/products/design-tools/vivado.html.
- GRMON3 debug monitor
- Workstation with Windows or Linux

Frontgrade Gaisler's standard offer of toolchains can be used to build and run software on the LEON3-XCKU-NANDFCTRL2-EX design. Toolchains and run-time environments are available for download via http://gaisler.com.

4.2 Programming the FPGA device and connecting with GRMON3

Please see the LEON3-XCKU-NANDFCTRL2-EX Quick Start Guide [QSG] for information on FPGA programming and using the SoC design.

4.3 Support

In case of technical issues please contact support@gaisler.com.

Sales and licensing questions should be directed to sales@gaisler.com.

5 Ordering information

Please contact sales@gaisler.com for information on the GRLIB IP library.

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