LEON-RTG4-EX

SPARC V8 Processor

2018 User's Manual

The most important thing we build is trust

Features

- SPARC V8 integer unit(s) with 7-stage pipeline, 8 register windows, 16 KiB instruction and 16 KiB data caches, hardware multiplier and divider, power-down mode, hardware watchpoints, etc.
- Double precision IEEE-754 floating point unit
- Memory management unit
- EDAC protected interface to DDR3 SDRAM
- Advanced on-chip debug support unit
- UART, Timers, GPIO port, Interrupt controller, Status registers
- Multiple SpaceWire links with RMAP CRC (option)
- Redundant 1553 BC/RT/MT interfaces (option)
- Redundant CAN 2.0 interfaces (option)
- Ethernet 10/100/1000 Mbit MAC interface (option)
- Level-2 cache (option)

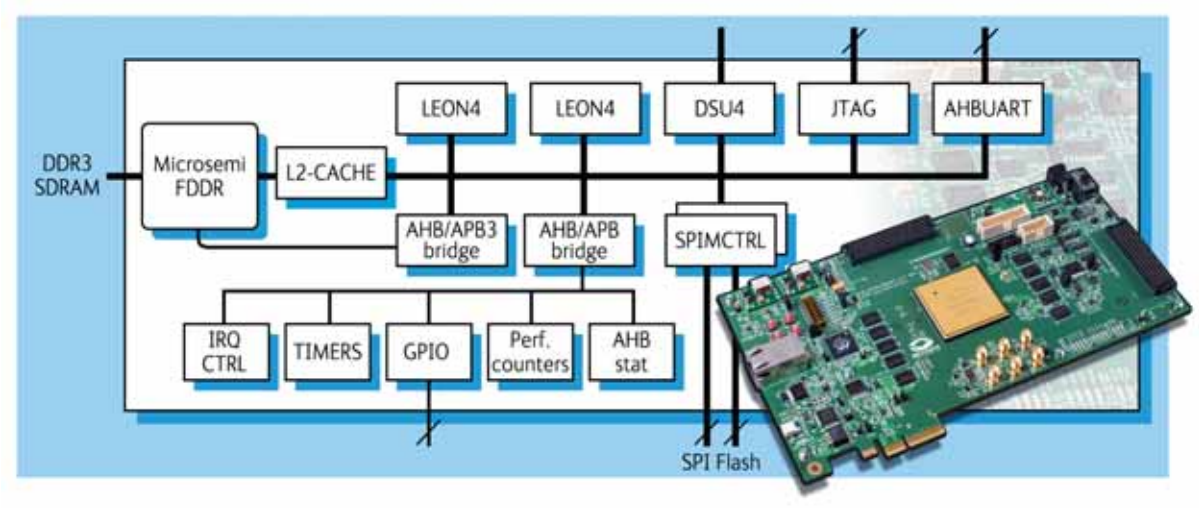
Description

The LEON-RTG4-ES FPGA bitstreams are a collection of example designs built from Cobham Gaisler's GRLIB IP library using a template design for Microsemi RTG4 devices. The example designs are suitable for evaluation of LEON3FT and LEON4FT microprocessors in RTG4 system-on-chip designs.

Specification

- Targets Microsemi RTG4 Development Kit FPGA board

- 50 MHz system frequency
- Up to 200MIPS, 200 MFLOPS



Applications

The LEON/GRLIB template designs can be adapted as multiple configurations, covering instrument, payload and control applications. The LEON-RTG4-EX example bitstreams are unsuitable for use in harsh environments.

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1 Introduction

1.1 Scope

The GRLIB IP library has support for Microsemi RTG4 devices. This support consists of a techmap layer that wraps RTG4 specific technology elements such as memory macros and pads. GRLIB also contains a template design for the RTG4 Development Kit, bridges that allow to use the Microsemi FDDR memory controller and SerDes IP together with a LEON/GRLIB system, and infrastructure that automatically builds project files for Libero SoC.

This document described a set of ready-made RTG4 FPGA configurations (bitstreams) that have been built from the GRLIB RTG4 template design.

1.2 Document revision history

Table 1. Change record

Version	Date	Note
1.0	2017 February	First issue
1.1	2017 February	Minor update
2.0	2018 May	Added new Introduction section. Move reference documents section. Update design descriptions to match 2018-05-08 versions of bitstreams (EX1 discontinued) Added sections on resource utilization and power consumption.
2.1	2018 May	Mark EX1 as discontinued in table of configurations.

1.3 Reference documents

[AMBA] AMBA^{TM} Specification, Rev 2.0, ARM IHI 0011A, 13 May 1999, Issue A, first release, ARM Limited

[GRLIB] GRLIB IP Library User's Manual, Cobham Gaisler, www.Cobham.com/gaisler

[GRIP] GRLIB IP Core User's Manual, Cobham Gaisler, www.Cobham.com/gaisler

[SPARC] The SPARC Architecture Manual, Version 8, Revision SAV080SI9308, SPARC International Inc.

2 Example designs

2.1 Overview

The LEON-RTG4-EX collection of example designs are based on a common architecture. The architecture is centered around the AMBA [AMBA] Advanced High-speed Bus (AHB), to which the LEON3 or LEON4 SPARC V8 [SPARC] processors and other high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge. The architecture for the basic design is shown in figure 1.

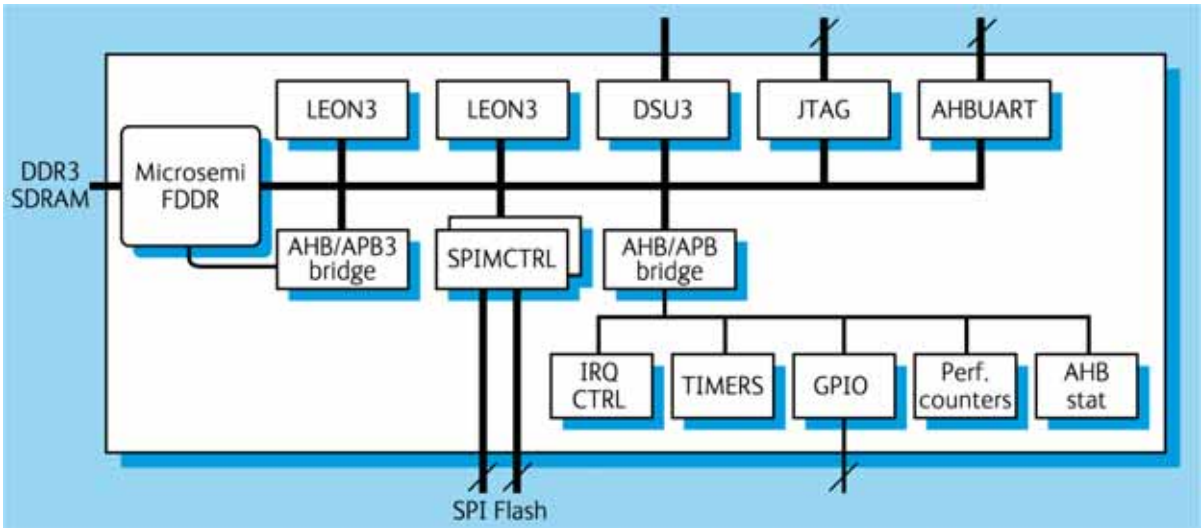

Figure 1. Architectural block diagram of LEON-RTG4-EX2

The full LEON-RTG4 architecture includes the following modules:

- LEON3FT or LEON4FT SPARC V8 Integer Unit with 16 KiB instruction cache and 16 KiB data cache. IEEE-754 Floating Point Unit and Memory Management Unit.
- Debug Support Unit with UART and JTAG Debug Links
- Bridge to Microsemi FDDR DDR3 SDRAM controller
- Timer unit with two 32-bit timers
- Interrupt controller for 15 interrupts in two priority levels
- UART with FIFO and separate baud rate generator
- General purpose I/O port (GPIO).
- AMBA AHB status register

There are also example variants that include a Level-2 cache controller. In this case the Level-2 cache is located between the FDDR memory controller and the rest of the system. The GRLIB IP library contains a template design for the Microsemi RTG4 Development Kit board. The example designs can easily be extended to add additional GRLIB IP library IP cores such as:

- 8/32-bit Memory Controller with EDAC for external PROM, SRAM and I/O
- 8/32-bit SDRAM Controller with EDAC for external PC100 SDRAM, PROM, SRAM and I/O
- SpaceWire links with CRC support and hardware RMAP target
- CAN-2.0 controllers
- Mil-Std-1553 BC/BM/RT
- Ethernet Media Access Controller (MAC)

A full list of GRLIB IP library components can be found in [GRIP]. The GRLIB user's manual is available on-line [GRLIB].

2.2 Configurations

Table 2 below lists the LEON-RTG4-EX example configurations. The bitstreams with example designs are intended to cover a wide range of application scenarios. For simple control where logic utilization needs to be kept low, the EX2 configuration can be used by running software on only one of the processor cores and avoiding use of the MMU and FPU. For applications that require more performance the EX3, EX4, EX5, and EX6 configurations are recommended.

The bitstreams are available for download from https://gaisler.com/LEON-RTG4

Table 2. Example configurations

Configuration name	**EX1**	**EX2**	**EX3**	**EX4**	**EX5**	**EX6**
RTG4 device	ES	**PROTO**	**PROTO**	**PROTO**	**PROTO**	**PROTO**
Processor	DISCONTINUED	LEON3	LEON3	LEON3	LEON4	LEON4
Number of processor cores		2	4	2	4	2
Level-1 cache		16+16 KiB	16+16 KiB	16+16 KiB	16+16 KiB	16+16 KiB
Hardware multiply&divide		Yes	Yes	Yes	Yes	Yes
Multiply & accumulate		No	No	No	No	No
Single-vector trapping		Yes	Yes	Yes	Yes	Yes
Power down mode		Yes	Yes	Yes	Yes	Yes
Memory Management Unit		Yes	Yes	Yes	Yes	Yes
Floating Point Unit		GRFPU-lite	GRFPU-lite	GRFPU	GRFPU-lite	GRFPU
Debug Support Unit		Yes	Yes	Yes	Yes	Yes
Level-2 cache		No	Yes	Yes	Yes	Yes
UART Debug Link		Yes	Yes	Yes	Yes	Yes
JTAG Debug Link		Yes	Yes	Yes	Yes	Yes
Ethernet MAC 10/100/1000 Mbit		No[1]	No[1]	No[1]	No[1]	No[1]
Memory Controller		FDDR and SPI Flash	FDDR and SPI Flash	FDDR and SPI Flash	FDDR and SPI Flash	FDDR and SPI Flash
Standard peripherals	Yes	Yes	Yes	Yes	Yes	Yes

[1] Ethernet has been disabled due to difficulties in meeting timing for the 125 MHz domains required for the Ethernet SGMII interface. Recommendation is to use GMII instead on this technology (not supported by RTG4 Development Kit board)

Note: The configurations above are examples on how to use the GRLIB IP cores on RTG4. All IP cores have several configuration parameters and are individually configurable.

Note: While software will report that fault-tolerance is enabled for the example designs, the bitstreams are not suitable for use in environments with radiation effects.

3 Architecture

3.1 Cores

The common architecture is based on cores from the GRLIB IP library. The vendor and device identifiers for each core can be extracted from the plug & play information. The used IP cores are listed in table 3.

Table 3. Used IP cores

Core	Function	Vendor	Device
AHBCTRL	AHB Arbiter & Decoder	0x01	-
APB3CTRL	AHB/APB3 Bridge	0x01	0x0A2
APBCTRL	AHB/APB Bridge	0x01	0x006
LEON3FT	LEON3 SPARC V8 32-bit processor	0x01	0x053
DSU3	LEON3 Debug support unit	0x01	0x004
L3STAT	LEON3 Performance counters	0x01	0x098
LEON4	LEON4 SPARC V8 32-bit processor	0x01	0x048
DSU4	LEON4 Debug support unit	0x01	0x049
L4STAT	LEON4 Performance counters	0x01	0x047
AHBUART	Serial/AHB debug interface	0x01	0x007
AHBJTAG	JTAG/AHB debug interface	0x01	0x01C
FTAHBRAM	On-chip SRAM with EDAC	0x01	0x050
AHBSTAT	AHB failing address register	0x01	0x052
APBUART	8-bit UART with FIFO	0x01	0x00C
GPTIMER	Modular timer unit with watchdog	0x01	0x011
IRQMP	LEON3 Interrupt controller	0x01	0x00D
GRGPIO	General purpose I/O port	0x01	0x01A
L2CACHE	Level-2 Cache Controller	0x01	0x04B
SF2MDDR	SF2/IGLOO2/RTG4 MDDR/HPMS bridge	0xAC	0x002 / 0x003
SPIMCTRL	SPI Memory controller	0x01	0x045

Note that the table above lists IP cores used in the full set of LEON-RTG4-EX designs. Several designs contain a subset of the IP cores in the table.

3.2 Interrupts

The LEON-RTG4-EX example designs use the same interrupt assignment for all configurations. See the description of the individual cores for how and when the interrupts are raised. All interrupts are handled by the interrupt controller and forwarded to the processor.

Table 4. Interrupt assignment

Core	Interrupt	Comment
AHBSTAT	7	
APBUART 0	2	
GPTIMER	8, 9	
SPIMCTRL0	10	
SPIMCTRL1	11	

3.3 Memory map

The example designs use the same memory map for all standard configurations. The memory map shown in table 5 is based on the AMBA AHB address space. An access to addresses outside the ranges will receive an AHB error response. The detailed register layout is defined in the description of each individual core.

Table 5. AMBA AHB address range

Core	Address range	Area
FDDRW	0x40000000 - 0x7FFFFFFF	DDR3 SDRAM area
APBCTRL	0x80000000 - 0x800FFFFF	APB bridge
DSU3	0x90000000 - 0x9FFFFFFF	Registers
APB3CTRL	0xB0000000 - 0xB00FFFFF	APB3 bridge
SPIMCTRL0	0xC0000000 - 0x07FFFFFF	SPI Flash area
SPIMCTRL1	0xC8000000 - 0x0FFFFFFF	SPI Flash area
SPIMCTRL0	0xFFF90000 - 0xFFF900FF	Registers
SPIMCTRL1	0xFFFA0000 - 0xFFFA00FF	Registers
AHB plug&play	0xFFFFF000 - 0xFFFFFFFF	Registers

The control registers of most on-chip peripherals are accessible via the AHB/APB bridge and the AHB/APB3 bridge that is mapped at address 0x80000000 and 0xB0000000, respectively. The memory map shown in table 6 is based on the AMBA AHB address space.

Table 6. APB address range

Core	Address range	Comment
APBUART	0x80000100 - 0x800001FF	
IRQMP	0x80000200 - 0x800002FF	
GPTIMER	0x80000300 - 0x800003FF	
AHBUART	0x80000700 - 0x800007FF	
GRGPIO	0x80000B00 - 0x80000BFF	
GRETH_GBIT	0x80000C00 - 0x80000CFF	
AHBSTAT	0x80000F00 - 0x80000FFF	
APB plug&play	0x800FF000 - 0x80100000	
FDDRE	0xB0002000 - 0xB00027FF	
APB3 plug&play	0xB00FF000 - 0xB0100000	

3.4 IP core documentation

This user manual does not contain IP core documentation. Please refer to the GRLIB IP Core User's Manual [GRIP] available at http://gaisler.com/products/grlib/grip.pdf.

The bitstream packages include the configuration files used to generate the different LEON-RTG4-EX example designs from the GRLIB template designs. These configuration files can be studied to determine how the IP cores have been configured, if not already explained by this user's manual. The GRMON debug monitor also provides information about the system-on-chip's configuration via the command **info sys**.

3.5 Signals

Please refer to the RTG4 Development Kit documentation for a description of the board. The LEON SoC design has the following signal maps:

- System reset status is mapped to LED0
- LEON processor error output is mapped to LED2
- DSU active output is mapped to LED3
- WDOG is mapped to LED4
- SERDES ready mapped to LED5 (active low)

The following control and bootstrap signals are mapped:

- DIP switch 1 on SW5 selects between APBUART and AHBUART
- DSU break is mapped to switch 2 (SW2)
- System reset is mapped to switch 7 (SW7)

3.6 Resource utilization

Resource utilization is described in the GRLIB area spreadsheet, available at:

https://www.gaisler.com/products/grlib/grlib_area.xls

3.7 Power consumption

The following power summaries are reported by Libero SoC 11.8-SP3:

Table 7. Power analysis results

Design	Total power (mW)	Static	Dynamic
EX3	1664	26%	74%
EX6	1469	30%	70%

4 Working with the board

4.1 Prerequisites

The following items are required to use LEON-RTG4-EX designs:

- Workstation with Windows or Linux
- RTG4 Development Kit
- LEON-RTG4-EX bitstream
- GRMON3 debug monitor

The two last items can be downloaded via http://gaisler.com/LEON-RTG4.

Cobham Gaislers standard offer of toolchains can be used to build and run software on the LEON-RTG4-EX designs. Toolchains and run-time environments are available for download via http://gaisler.com.

4.2 Programming the FPGA device

The FPGA needs to be programmed with a LEON-RTG4-EX bitstream. A bitstream package is available at https://gaisler.com/LEON-RTG4 and the designs are arranged in subdirectories after their name. The example design subdirectory contains a FlashPro Express (FPExpress) job that should be loaded in the tool. The FPGA is then programmed by pressing the RUN button in FlashPro Express.

NOTE: Previous versions of the LEON-RTG4-EX bitstream package contained a bitstream for the RTG4_ES development kit. The EX1 bitstream has been discontinued and the bitstreams can only be used with PROTO devices.

4.3 Connecting with GRMON3

The GRMON3 debug monitor can be used to connect to the board. The recommended way is to use the on-board FTDI device. In this case the jumpers J32 and J27 need to be set to 1-2 on the board. GRMON should then be started with the -ftdi flag.

It is possible to use the GRMON3 evaluation version with the LEON-RTG4-EX designs.

When GRMON3 connects to the board it will automatically initialize the designs peripherals, including the DDR3 SDRAM controller. The debug monitor performs the same functions that would be performed by a bootloader in standalone operation of a LEON/GRLIB system.

4.4 Support

In case of technical issues please contact support@gaisler.com. The support line is normally available only to companies and institutions with active support contracts. Limited support for the LEON-RTG4-EX example designs is provided. When contacting support please provide a clear description of which design that is used and your affiliation.

Sales and licensing questions should be directed to sales@gaisler.com.

5 Ordering information

Please contact sales@gaisler.com for information on the GRLIB IP library.

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