Examples of Core Supply Power Consumption of the GR712RC

Technical note

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1 INTRODUCTION

1.1 Scope of the Document

Power consumption of a microprocessor is in general highly dependent on a number of use-case specific parameters. Supply voltage, operating frequency and resource utilization, i.e. effects of the type of software executing on the device, are major contributing factors. This technical note intends to complement data sheet values of typical core power consumption of the GR712RC device, based on various application examples.

The work has been performed by Cobham Gaisler AB, Göteborg, Sweden.

1.2 Reference Documents

[RD1] "Dual-Core LEON3-FT SPARC V8 Processor, GR712RC, Data Sheet", January 2016, Issue 2.3, link

2 ABBREVIATIONS

AMP	Asymmetric Multi-Processing
CPU	Central Processing Unit
DMA	Direct Memory Access
DUT	Device Under Test
FPU	Floating-Point Unit
RCC	RTEMS Cross-Compiler system
SPI	Serial Peripheral Interface
SpW	SpaceWire
UART	Universal Asynchronous Receiver/Transmitter

3 POWER DISSIPATION MEASUREMENT TEST CASES

3.1 Test case specification

Test cases are defined in the following format:

Name	Description
Identifier	Name which uniquely identifies the test case.
Description	A brief description of the test case operation.
Operation	A sequence of operations performed on the DUT. The description is written in high level English. Operations on memory and registers are typically performed using GRMON2.

Each test case was run at different system clock speeds, additionally varying the supply voltage by +10% and -10% of the nominal value. Results of power measurement are given in chapter 4. The same data is also provided in a separate spreadsheet. Values are mean values once operation on the DUT entered a steady state.

3.2 Description of test cases

Identifier	100
Description	System inactive power test
Preparation	The RCC-1.2 rtems-tasks in AMP configuration with disabled printouts.
Operation	• Minimal I/O accesses (no SPI, UART, SpW .. communication) • Minimal memory accesses • Minimal CPU usage (both CPUs in power-down)

Identifier	101
Description	Processor 0 load power test
Operation	• Minimal I/O accesses (no SPI, UART, SpW .. communication) • Minimal I/O DMA accesses • Minimal CPU1 usage (CPU1 in power-down) • Utilize CPU0 100% with integer code only • Minimal CPU0 memory accesses (I-cache hits, D-cache read hits, no data writes)

Identifier	102
Description	Processors 0 and 1 load power test
Operation	• Minimal I/O accesses (no SPI, UART, SpW .. communication) • Minimal I/O DMA accesses • Utilize CPUs 100% with integer code only • Minimal CPUs memory accesses (I-cache hits, D-cache read hits, no data writes)
Note	• Similar to test 101 but with both CPUs active

Identifier	103
Description	Processors 0 FPU load power test
Operation	• Minimal I/O accesses (no SPI, UART, SpW .. communication) • Minimal I/O DMA accesses • Minimal CPU1 usage (CPU1 in power-down) • Utilize CPU0 100% with FPU instruction code • Minimal CPUs memory accesses (I-cache hits, D-cache read hits, no data writes)

Identifier	110
Description	Processor frequency test
Operation	• Prepare system for executing the Dhrystone test case.

Identifier	111
Description	RAM memory test
Operation	• Perform an exhaustive memory test (RAM space) where different access patterns are performed, including long bursts of read/write accesses and accesses over memory bank borders.

Identifier	112
Description	PROM memory test
Operation	• Perform an exhaustive memory test (PROM space) where different access patterns are performed, including long bursts of read/write accesses and accesses over memory bank borders.

Identifier	120a
Description	SpaceWire 100 Mbit/s power test
Operation	• Perform transfer of data from SPW link A to SPW link B, and vice versa, using the driver initialized with 128 RX buffers with size of 256 byte. • Compare sent data with received data.

Identifier	120b
Description	SpaceWire 40 Mbit/s power test
Operation	• Perform transfer of data from SPW link A to SPW link B, and vice versa, using the driver initialized with 128 buffers with size of 256 byte. • Compare sent data with received data.

Identifier	130
Description	SpaceWire 100 Mbit/s error-reset state power test
Operation	• Disable all cores except for SpaceWire cores 0 and 1 by using the clock gating unit. • Configure SpaceWire cores 0 and for 100 Mbit/s but do not establish a link (do not enter run state).

Identifier	131
Description	SpaceWire 100 Mbit/s run state power test
Operation	• Disable all cores except for SpaceWire cores 0 and 1 by using the clock gating unit. • Configure SpaceWire cores 0 and for 100 Mbit/s and establish a link (enter run state).

Identifier	132
Description	SpaceWire 40 Mbit/s run state power test
Operation	• Same as test 131 but with 40 Mbit/s bit rate

Identifier	140
Description	RAM memory 64-bit write stress test
Operation	• Perform many 64-bit write operations to different location of the RAM Memory. The memory shall be written by the CPU using std instructions.

Identifier	141
Description	RAM memory 64-bit read stress test
Operation	• Perform many 64-bit read operations to different location of the RAM Memory. The memory shall be read by the CPU using ldd instructions.

4 POWER DISSIPATION MEASUREMENT RESULTS

Measurements were taken using a Texas Instruments INA219 Current/Power Monitor with a 0.02 Ω current-shunt resistor in the GR712RC core supply path. Figures in the tables below are in [mW]:

Voltage	Nominal (1.8V)			
Frequency/MHz	24	50	64	80
test100	140	242	294	358
test101	286	524	656	802
test102	426	806	1010	1236
test103	258	484	602	738
test110	292	544	678	832
test_mem 111	292	544	692	848
test_mem 112	266	502	622	764
test120a	348	620	756	914
test120b	406	668	810	966
test130	222	374	456	548
test131	230	380	462	554
test132	292	442	522	612
test_mem 140	380	632	766	918
test_mem 141	370	610	738	882

Voltage	Min (1.62V)			
Frequency/MHz	24	50	64	80
test100	114	196	240	288
test101	226	430	530	648
test102	338	656	816	1002
test103	210	390	488	596
test110	232	440	584	672
test_mem 111	236	446	558	684
test_mem 112	216	404	504	616
test120a	282	498	612	740
test120b	328	544	656	780
test130	180	302	368	446
test131	184	308	374	448
test132	236	358	422	494
test_mem 140	308	512	622	740
test_mem 141	298	494	596	714

Voltage	Max (1.98V)			
Frequency/MHz	24	50	64	80
test100	170	292	358	432
test101	338	632	790	966
test102	504	970	1216	1488
test103	312	584	728	892
test110	350	656	820	1000
test_mem 111	350	668	832	1020
test_mem 112	322	602	750	920
test120a	420	744	914	1102
test120b	488	810	976	1164
test130	268	452	550	662
test131	278	458	558	668
test132	350	534	630	740
test_mem 140	458	764	924	1108
test_mem 141	446	738	888	1062