GR712RC-BOARD Letter of Volatility

Letter of Volatility 2023-09-27

Doc. No GR712RC-BOARD-LOV

Issue 1.0

CHANGE RECORD

Issue	Date	Section / Page	Description
1.0	2023-09-27	All	First issue of this document.

1 INTRODUCTION

1.1 Scope of the document

This document is a Letter of Volatility for the GR712RC-BOARD development board [RD1]. It applies to revision 0.3 and earlier of the product.

1.2 Reference documents

[RD1] GR712RC-BOARD user's manual, https://gaisler.com/index.php/products/boards/gr712rc-board

[RD2] GRMON3-UM,"GRMON3 User's Manual", https://gaisler.com/doc/grmon3.pdf

[RD3] GR712RC-UM, "GR712RC User's Manual", https://gaisler.com/gr712rc

1.3 Abbreviations

b	Bit
B	Byte (8 bits)
EEPROM	Electrically Erasable Programmable Read-Only Memory
I2C	Inter-Integrated Circuit
Ki	Kibi (2^{10}=1024)
Mi	Mebi (2^{20}=1048576)
PID	Product ID
RAM	Random Access Memory
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SODIMM	Small Outline Dual In-Line Memory Module
SPD	Serial Presence Detect
SRAM	Static Random Access Memory
USB	Universal Serial Bus
VID	Vendor ID

1.4 Terms and Definitions

Power off: To remove the external 5 V power input from the board and keep it removed for a minimum of 10 s.

Volatile memory: Memory that requires external power to retain its contents.

Non-volatile memory: A memory that retains its contents without an external source of power.

User Accessible memory: A memory that can be written by use of the GRMON debug software [RD2] or user application software running inside the GR712RC [RD3].

2 SUMMARY

2.1 Volatile memory

Device/Function	Type	Size	User Accessible	Sanitization Procedure
GR712RC internal memory (L1-cache, local RAM, registers)	SRAM and flip-flops	<2.1 MiB	Yes	Power off
External RAM for GR712RC	SODIMM SDRAM	256 MiB	Yes	Power off
External RAM for GR712RC	SRAM	10 MiB	Yes	Power off
FT2232HHL USB-JTAG converter	Internal RAM		No	Power off

All volatile memory on the GR712RC-BOARD can be erased by removing 5 V power from the board for a time of 10 s or longer. The board does contain a power source in the form of a small battery for the RTC (see next section), but this battery is not capable of powering any other device on the board.

2.2 Non-volatile memory

Function	Type	Size	User Accessible	Sanitization procedure
Boot memory for GR712RC	Flash	8 MiB	Yes	Section 1
RTC counter	Battery-backed volatile memory	32 b	Yes	Section 2.4
SODIMM SPD parameters	EEPROM	128 B	No	None
FT2232HL configuration parameters[1]	EEPROM	128 B	No[2]	None

1. Only present on revision 0.3 and later of the GR712RC-BOARD.
2. Not User Accessible per section 1.4, but reprogrammable with commonly available software and hardware. For default contents at delivery see section 3.6.

2.3 Sanitization procedure for GR712RC boot memory

Prerequisites: GRMON2 or GRMON3 debug software [RD2]

For information about the function and location of each jumper referenced in the below procedure, refer to section 4.3 in [RD1].

1. Ensure that JP77 and JP83 are open (no jumper installed).
2. Ensure that position 5-6 on JP76 is closed (jumper installed).
3. Apply power to the board.
4. Connect the GRMON debug monitor software to the GR712RC-BOARD using any supported debug link. For details refer to section 4.15 in [RD1].
5. In the GRMON command prompt run the commands "`flash`", "`flash unlock all`", and "`flash erase all`".

After erasure, the flash will contain the value 0xFF on all byte addresses. The expected output from GRMON3 is shown below:

```
grmon3> flash

  Intel-style 8-bit flash on D[31:24]

  Manuf.        : Intel
  Device        : MT28F640J3
  Device ID     : a6ff27a4002c0c58
  User ID       : ffffffffffffffff

  1 x 8 Mbytes = 8 Mbytes total @ 0x00000000

  CFI information
  Flash family  : 1
  Flash size    : 64 Mbit
  Erase regions : 1
  Erase blocks  : 64
  Write buffer  : 32 bytes (limited to 32)
  Lock-down     : Not supported
  Region  0     : 64 blocks of 128 kB

grmon3> flash unlock all
  Unlock in progress
  Block @ 0x007e0000 : code = 0x80  OK
  Unlock complete

grmon3> flash erase all
  Erase in progress
  Block erase @ 0x007e0000 : code = 0x80  OK
  Erase complete

grmon3> mem 0x00000000
  0x00000000  ffffffff  ffffffff  ffffffff  ffffffff    ................
  0x00000010  ffffffff  ffffffff  ffffffff  ffffffff    ................
  0x00000020  ffffffff  ffffffff  ffffffff  ffffffff    ................
  0x00000030  ffffffff  ffffffff  ffffffff  ffffffff    ................
```

2.4 Sanitization procedure for the RTC

Prerequisites: GRMON2 or GRMON3 debug software [RD2]

1. Place JP57 and JP58 in position E to connect the GR712RC to the RTC I2C interface.
2. Install jumpers in position 1-2 and 3-4 on JP70 to enable pull-ups on the SDA and SCL lines.
3. Apply power to the board.
4. Connect the GRMON debug monitor software to the GR712RC-BOARD using any supported debug link. For details refer to section 4.15 in [RD1].
5. Ensure the RTC is responding to I2C accesses by running the command "`i2c scan`" in GRMON. GRMON should report one I2C slave at address 0x68.
6. Read the RTC counter value and internal settings with the command "`i2c read 0x68 0 6`".
7. Overwrite the counter with the value 0x00000000, disable the counter and disable trickle-charging using the commands below:
   ```
   i2c write 0x68 0 0x00
   i2c write 0x68 1 0x00
   i2c write 0x68 2 0x00
   i2c write 0x68 3 0x00
   i2c write 0x68 4 0x80
   i2c write 0x68 5 0x00
   ```
8. Verify that the write took effect by again reading the counter value and settings with the command "`i2c read 0x68 0 6`".

The expected output from GRMON3 is shown below. In this example, the initial RTC counter value was 0x6513f8bb, and the counter and trickle-charging was enabled.

```
grmon3> i2c scan
  Scanning 7-bit address space on I2C bus:
  Detected I2C device at address 0x68

  Scan of I2C bus completed. 1 device found

grmon3> i2c read 0x68 0 6
  00:  bb f8 13 65
  04:  00 ab

grmon3> i2c write 0x68 0 0x00
grmon3> i2c write 0x68 1 0x00
grmon3> i2c write 0x68 2 0x00
grmon3> i2c write 0x68 3 0x00
grmon3> i2c write 0x68 4 0x80
grmon3> i2c write 0x68 5 0x00

grmon3> i2c read 0x68 0 6
  00:  00 00 00 00
  04:  80 00
```


3 DETAILED DESCRIPTION

3.1 SDRAM SODIMM

The GR712RC-BOARD comes with a detachable SODIMM module providing external RAM for the GR712RC. This SODIMM is equipped with 256 MiB of volatile SDRAM and 128 B of non-volatile SPD EEPROM. The SDRAM is User Accessible and normally appears at address 0x60000000-0x7FFFFFFF in the GR712RC memory map. The memory can be erased by powering off the board.

The SPD EEPROM is not user accessible per the definition in section 1.4. However, the EEPROM could in theory be written by unplugging the SODIMM from the GR712RC-BOARD and connecting it to a custom I2C controller.

3.2 SRAM (CY7C1069)

On the GR712RC-BOARD are mounted 5 copies of the CY7C1069 SRAM IC, each of which has a capacity of 2 MiB. Optionally an additional 5 chips can be mounted on the bottom side of the board.

This memory is User Accessible and normally appears at address 0x40000000-0x5FFFFFFF in the GR712RC memory map. The memory can be erased by powering off the board.

3.3 GR712RC

A single GR712RC ASIC [RD3] is mounted on the board. It contains volatile memory in the form of (approximately) 280 KiB of SRAM (most of which forms the L1-caches and AHBRAM) and a smaller number of flip-flops. This memory can be erased by powering off the board. The GR712RC does not contain any non-volatile memory.

3.4 Boot PROM for GR712RC (28F640J3)

An 8 MiB non-volatile flash memory (28F640J3) is mounted on the board and connected to the GR712RC. This component provides a boot PROM for the GR712RC. See section 4.5 “Memory” in [RD1] for more information.

This non-volatile memory is User Accessible, and a sanitization procedure is provided in section 2.3.

3.5 Real Time Clock (DS1672)

The GR712RC-BOARD is fitted with a single DS1672 real-time clock which contains a single 32-bit counter and two 8-bit control registers. The counter is User Accessible through an I2C-interface connected to the GR712RC. Furthermore, the board is fitted with a backup battery connected to the DS1672 which effectively makes the counter non-volatile. A sanitization procedure is provided in section 2.4.

The backup battery is implemented with a 1.0 F supercapacitor which by default is discharged on delivery. When the supercapacitor is discharged, the RTC will not retain its state while the board is powered off and its counter will have an unpredictable value on power up. Trickle-charging of the supercapacitor can be enabled in the DS1672 via its I2C interface.

3.6 FT2232HL USB-JTAG converter and configuration EEPROM

The board features a FT2232HL chip that provides access to the GR712RC JTAG interface via the front-panel USB port. In board revision 0.3 and later, a 128 B EEPROM is connected to this device. In revision 0.2 and earlier, no EEPROM is present.

Neither the FT2232HL, nor the EEPROM connected to it are User Accessible per the definition in section 1.4. However, the EEPROM can be reprogrammed from any computer connected to the USB port of the GR712RC-BOARD. If that computer has the appropriate software installed.

At delivery the EEPROM is programmed with the following settings:

USB VID:PID: `0403:6010` (FTDI Default)

Manufacturer: "`Frontgrade Gaisler AB`"

Product Description: "`GR712RC-BOARD`"

Serial Number: "`GR712Bnnnn`", where "*nnnn*" is the 4-digit serial number of the board.

